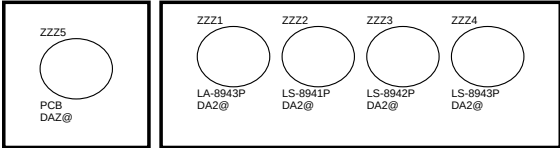


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Model Name : Q1VZC
File Name :LA-8943P
BOM P/N:43



Compal Confidential

CHROME M/B Schematics Document

Intel Sandy Bridge ULV Processor + Panther Point PCH

2012-08-10

REV:1.0

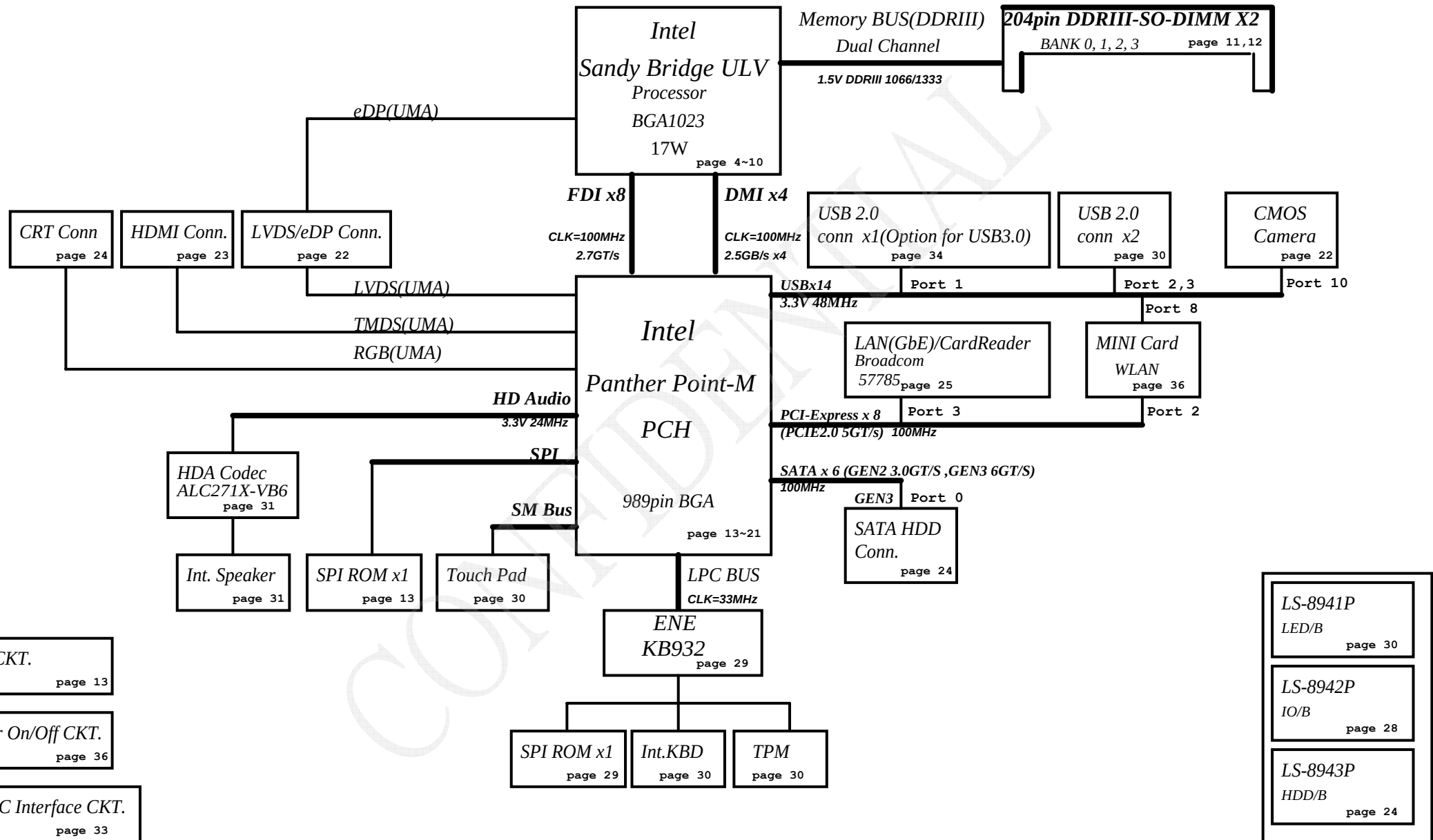
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Model Name : Q1VZC

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				Custom	4019K2
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				Sheet	2 of 45
				Rev	C

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON
+VCCSUS3_3	+3VALW to +VCCSUS3_3 power rail for PCH (Short Jump)	ON	ON	OFF
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON
+5VREF_SUS	+5VALW to +5VREF_SUS power rail for PCH (Short resister)	ON	ON	OFF
+5VS	+5VALW to +5VS switched power rail	ON	ON	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

PCH SM Bus address

Device	Address
ChannelA DIMM0 A0	1010 000X JDIMM1(STD)
ChannelB DIMM0 B0	1010 010X JDIMM2(REV)

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STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5(Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

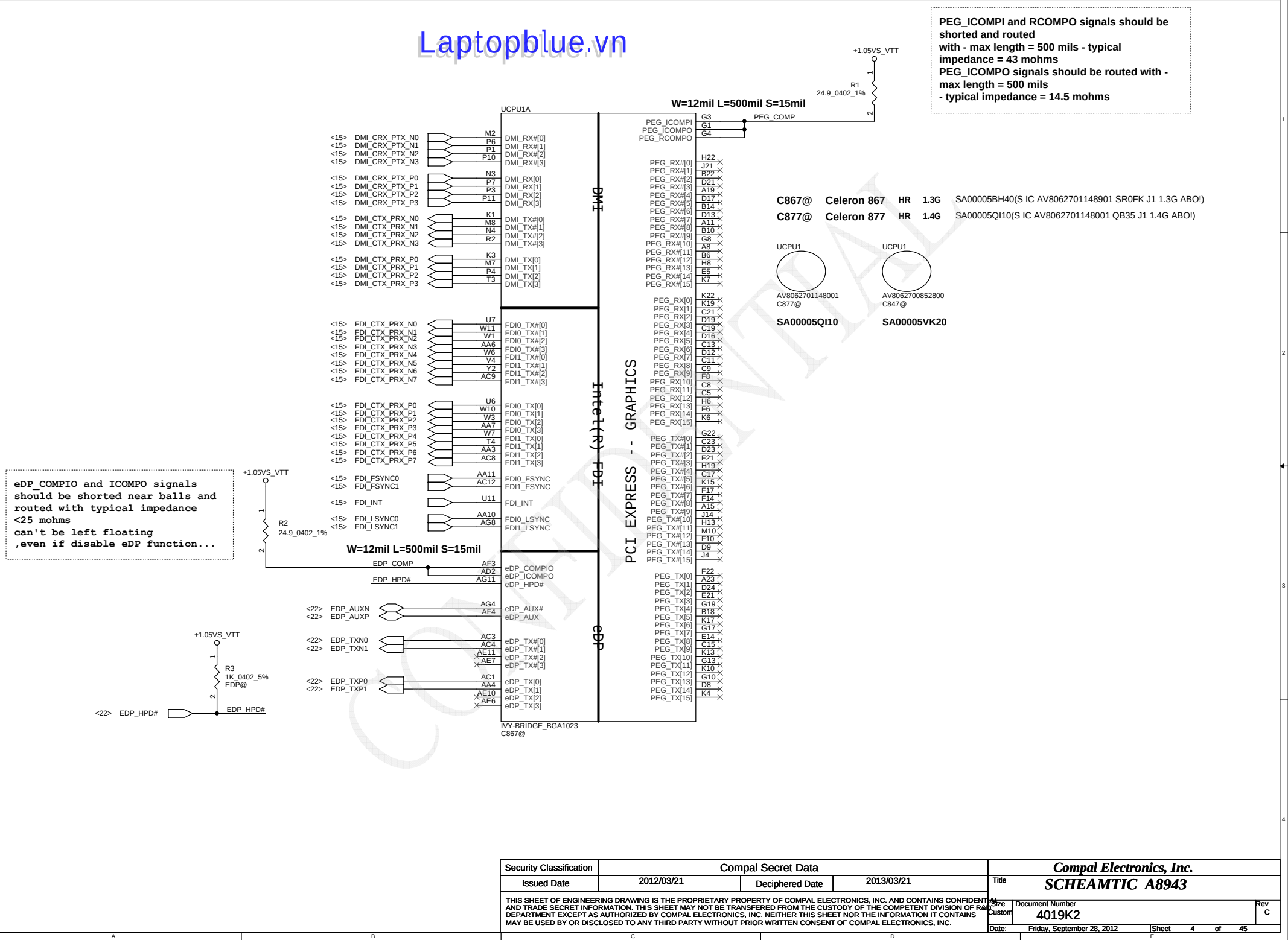
USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	
		1	USB 2.0(Options for USB3.0)
		2	USB port(Left 2.0)
	UHCI1	3	USB Port(Left 2.0)
		4	
		5	
EHCI2	UHCI2	6	
		7	
		8	Mini Card(WLAN)
	UHCI3	9	
		10	Camera
		11	
	UHCI4	12	
		13	

BTO Option Table

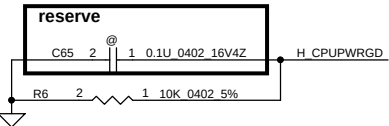
BTO Item	BOM Structure
Celeron 867	C867@
Celeron 877	C877@
Unpop	@
eDP Panel	EDP@
LVDS Panel	LVDS@
Connector	CONN@
USB3 Only	USB3@
Deep S3	DS3@
Normal S3	S3@
Intel i5/i7 CPU only	I57@
Celeron/Pentium/i3 CPU only	CP3@

USB 3.0	Port	
XHCI	1	
	2	USB Port(Right 3.0)
	3	
	4	

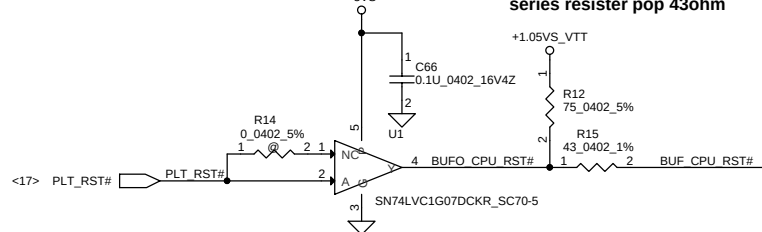


PCH->CPU
UNCOREPWRGOOD:非CORE外的電OK
SM_DRAMPWROK:DRAM power ok
RESET#:都ok後請CPU做reset

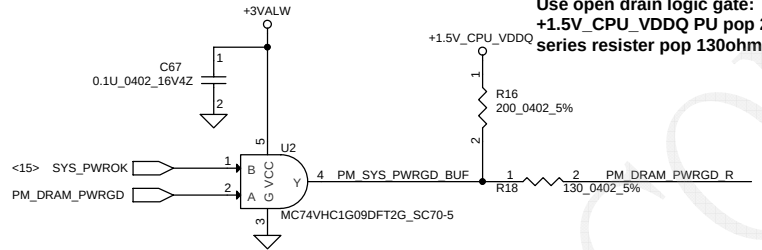
Follow DG 1.5 & Tacoma_Fall2 1.0



Follow DG 1.5 & Tacoma_Fall2 1.0
Buffered reset to CPU



Follow DG 1.5 & Tacoma_Fall2 1.0



PROC_SELECT#
PH VCPLL and connect to PCH DF_TV5

偵測CPU有無安裝

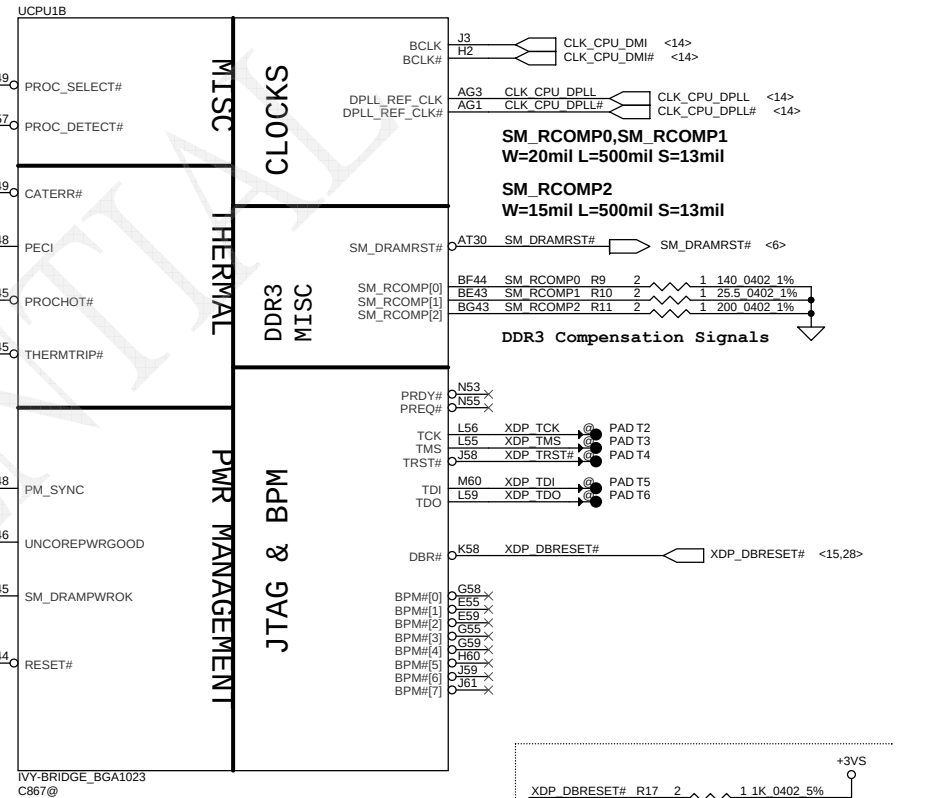
XBOX 三紅功能

follow Checklist 1.5

UNCOREPWRGOOD:非CORE外的電OK

SM_DRAMPWROK:DRAM power ok

12/22 Add(ESD request)



0921 LVDS@->@

CLK_CPU_DPLL# R4 2 LVDS@ 1 1K 0402 5%

CLK_CPU_DPLL R5 2 LVDS@ 1 1K 0402 5%

Checklist1.5 P.67 Graphis Disable Guide

eDP disable:

DPLL_REF_SSCLK PD 1K 5% to GND

DPLL_REF_SSCLK# PU 1K 5% to +1.05VS_VTT

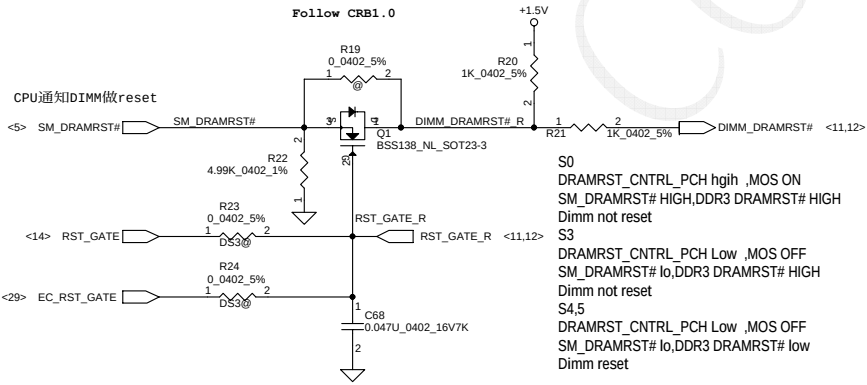
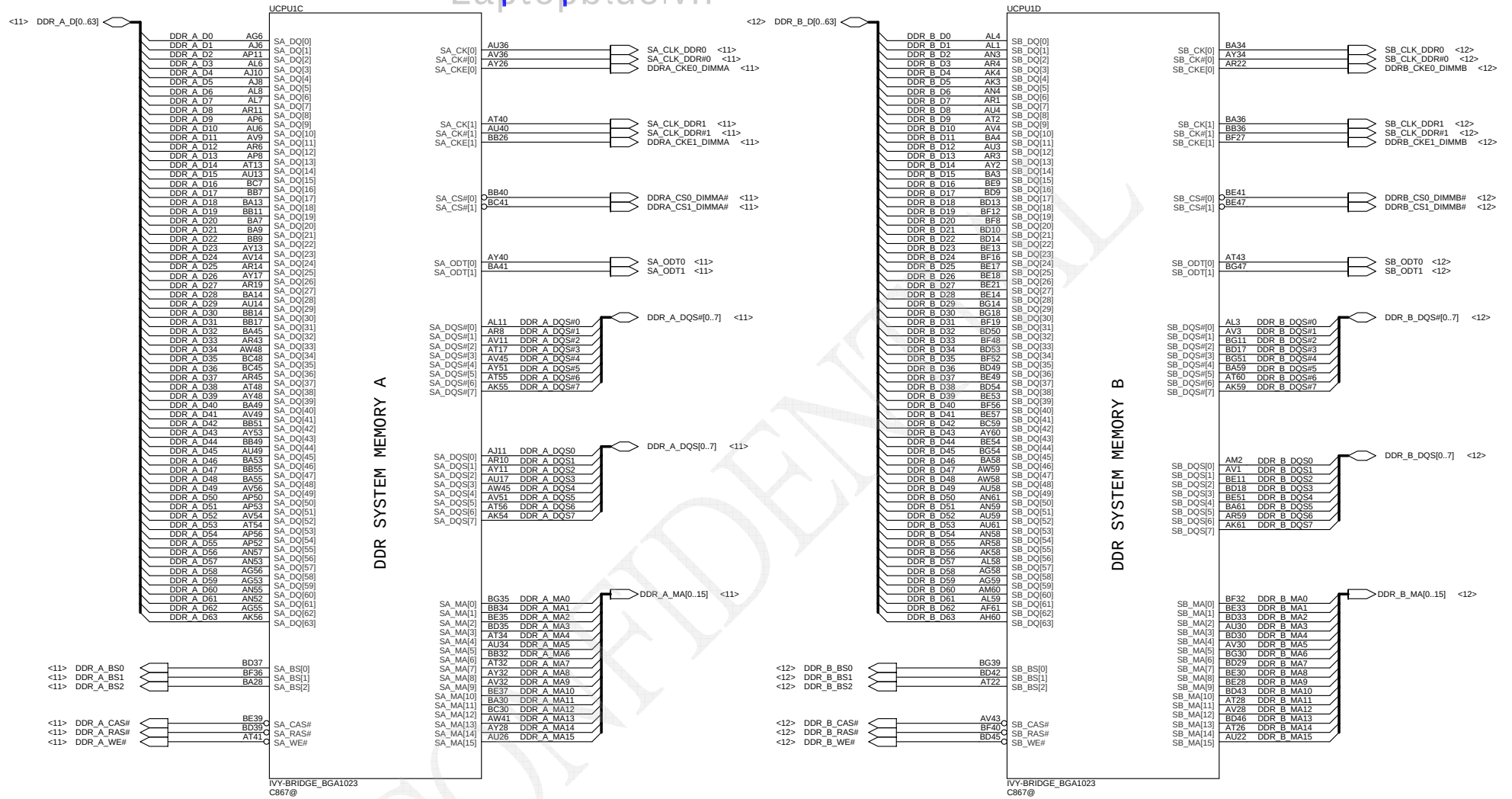
SM_RCOMP0,SM_RCOMP1
W=20mil L=500mil S=13mil

SM_RCOMP2
W=15mil L=500mil S=13mil

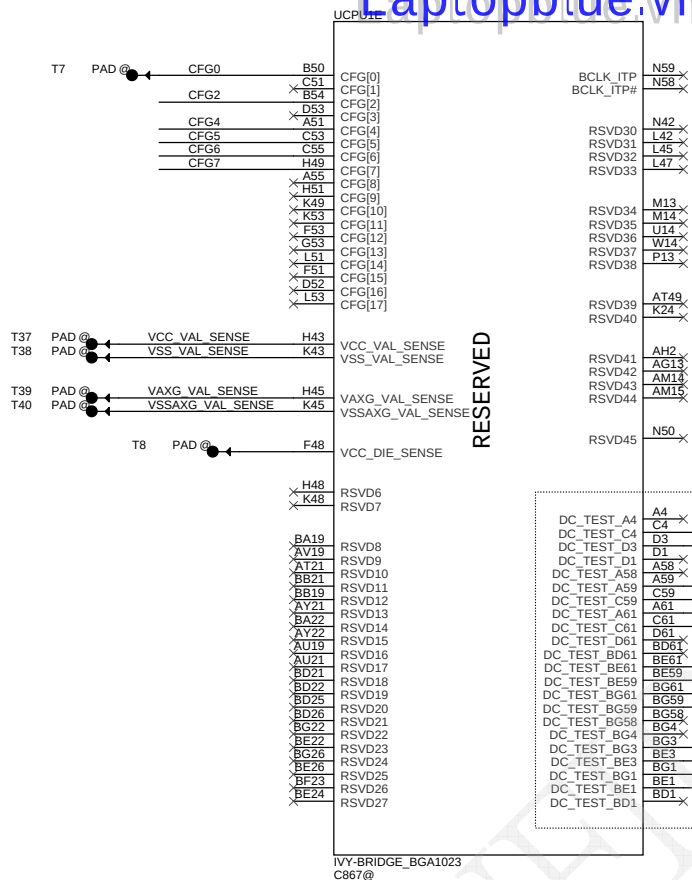
DDR3 Compensation Signals

Tacoma_Fall2 1.0 PU 1K +3VS
Check list 1.5 PU 1K +3VS
Debug port DG1.1-1.3 50-5K ohm

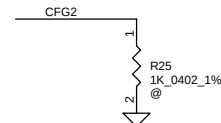
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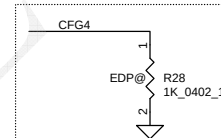


CFG Straps for Processor



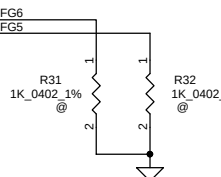
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0: Lane Reversed
------	--

UMA,Optimus eDP啟動
DISO eDP關閉

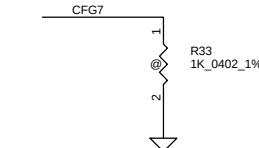
eDP enable

CFG4	★ 1: Disable 0: Enable
------	---------------------------



PCIe Port Bifurcation Straps

CFG[6:5]	11: (Default) 1x16 PCI Express ★ 10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express
----------	--



PEG DEFER TRAINING

Tacoma_Fall2 1.0 P.12

CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
------	---

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INTEL Recommend VCC
4*470UF,12*22uF(0805) and 35*2.2uF(0402)
PD0.8
CAP at P.51

POWER

8. 5A

UCPU1F

ULV type
06 33A

CORE SUPPLY

PEG IO AND DDR IO

VCCIO[1] AF46
VCCIO[3] AG48
VCCIO[4] AG50
VCCIO[5] AJ17
VCCIO[6] AJ21
VCCIO[7] AJ25
VCCIO[8] AJ43
VCCIO[9] AJ47
VCCIO[10] AK20
VCCIO[11] AK51
VCCIO[12] AL14
VCCIO[13] AL15
VCCIO[14] AL16
VCCIO[15] AL20
VCCIO[16] AL22
VCCIO[17] AL26
VCCIO[18] AL45
VCCIO[19] AL48
VCCIO[20] AM16
VCCIO[21] AM17
VCCIO[22] AM21
VCCIO[23] AM43
VCCIO[24] AM47
VCCIO[25] AN20
VCCIO[26] AN42
VCCIO[27] AN45
VCCIO[28] AN45
VCCIO[29] AM48

VCCIO[30] AA14
VCCIO[31] AB17
VCCIO[32] AB17
VCCIO[33] AC13
VCCIO[34] AD16
VCCIO[35] AD18
VCCIO[36] AD21
VCCIO[37] AE14
VCCIO[38] AE15
VCCIO[39] AF16
VCCIO[40] AF18
VCCIO[41] AF20
VCCIO[42] AG15
VCCIO[43] AG16
VCCIO[44] AG17
VCCIO[45] AG20
VCCIO[46] AG21
VCCIO[47] AJ14
VCCIO[48] AJ15
VCCIO[49] AJ15

VCCIO[50] W16
VCCIO[51] W17

VCCIO_SEL BC22 VCCIO_SEL

QUIET
RAILS

SVID

SENSE LINES

VCCPQE[1] AM25
VCCPQE[2] AN22

VIDALERT# R43
VIDCLK R43
VIDSOUT C44

VCC_SENSE R42
VSS_SENSE R43

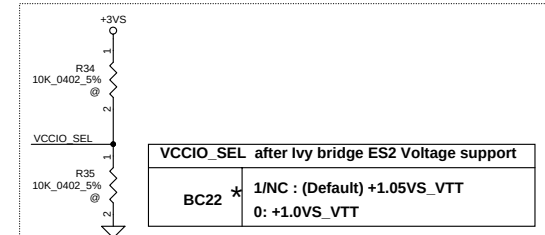
VCCIO_SENSE AN16
VSS_SENSE_VCCIO AN17

+1.05VS_VTT

For DDR

INTEL Recommend VCCIO
2*330UF,10*10uF(0603) and 26*1uF(0402)
PD0.8
CAP at P.51

For PEG



+1.05VS_VTT

+1.05VS_VTT

+1.05VS_VTT

R36 130_0402_5%

R37 75_0402_5%

Place the PU resistors close to CPU

R38 43_0402_1%
R39 2_0_0402_5%
R40 2_0_0402_5%

SVID_ALERT# <41>
SVID_CLK <41>
SVID_DATA <41>

Place the PU resistors close to VR

R41 100_0402_1%

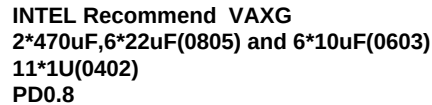
R42 10_0402_5%
R43 10_0402_5%

Should change to connect form power cirucit & layout differential with VCCIO_SENSE.

Check list 1.5

IVY-BRIDGE_BGA1023
C867@

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Customer				4019K2
Date: Friday, September 28, 2012				Rev C
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+V_SM_VREF should have 20 mil trace width

SA_DIMM_VREFDQ
SB_DIMM_VREFDQ
Check list1.5 P18 M1 default M3 no stuff

INTEL Recommend VDDQ
1*330uF,8*10uF(0603) ,10*1uF(0402)
PD0.8

SGA20331E10 S POLY C 330U
2V Y D2 LESR9M EEFSX H1.9

**INTEL Recommend VCCPLL
1*330uF,2*1uF(0402)
PD0.8**

```
<41> VCC_GFXSENSE
<41> VSS_GFXSENSE
```

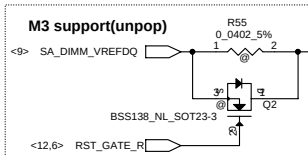
CR CheckList Rev1.5

1.2A

6A

INTEL Recommend VCCSA
1*330uF,5*10uF(0603) ,5*1uF(0402)
PD0.8

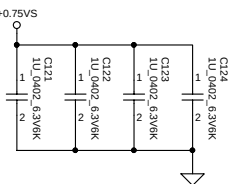
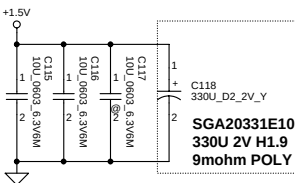
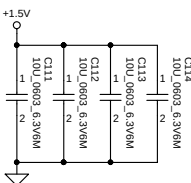
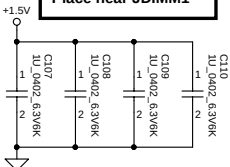
VCCSA				
VID0	VID1	Vout	HR	CR
0	0	0.9V	V	V
0	1	0.85V	V	V
1	0	0.775V	X	V
1	1	0.75V	X	V



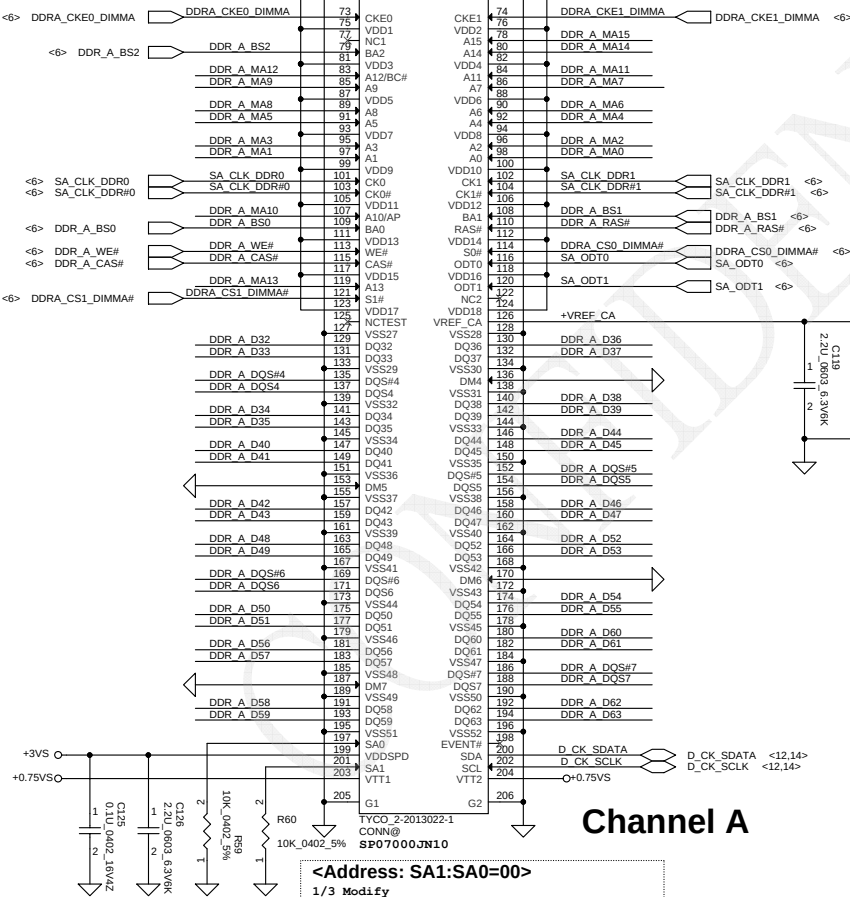
DDR_A_DQS#0[.7] <6>
DDR_A_DQS#0[.7] <6>
DDR_A_D[0.63] <6>
DDR_A_MA[0.15] <6>

Layout Note:
Place near JDIMM1

All VREF traces should
have 10 mil trace width



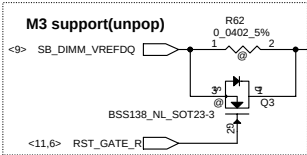
Layout Note:
Place near JDIMM1.203,204



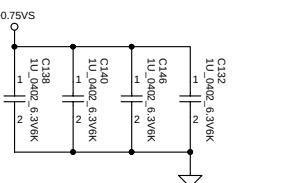
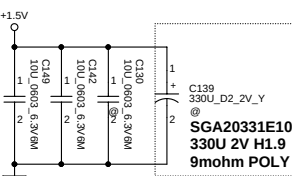
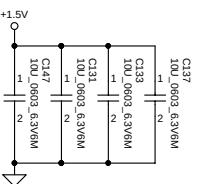
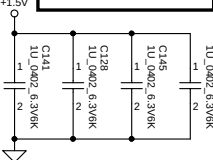
Channel A

<Address: SA1:SA0=00>
1/3 Modify
DIMM_1 Standard H:4.0mm

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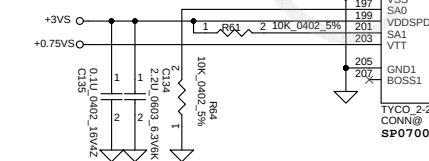
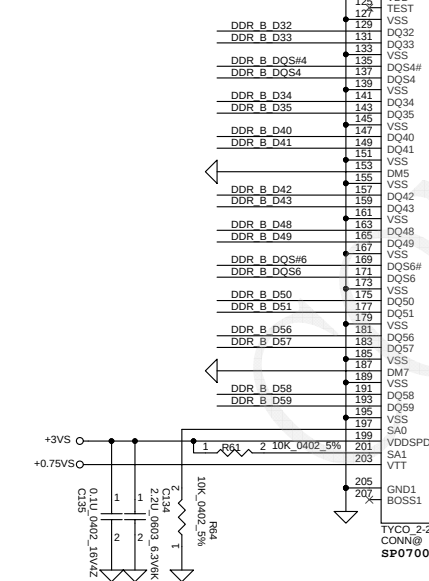
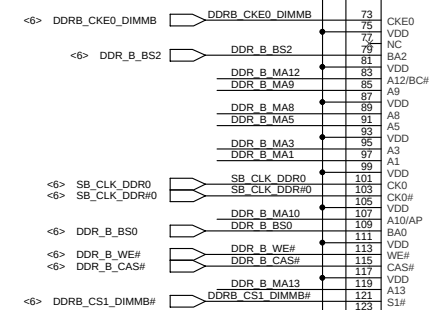


Layout Note:
Place near JDIMM2



Layout Note:
Place near JDIMM2.203,204

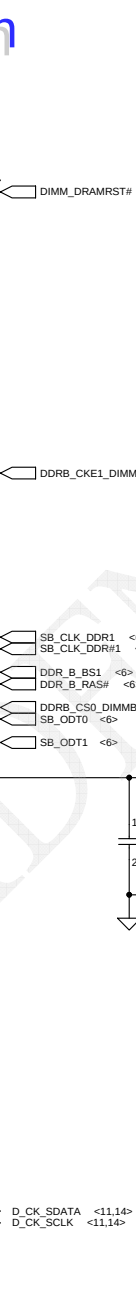
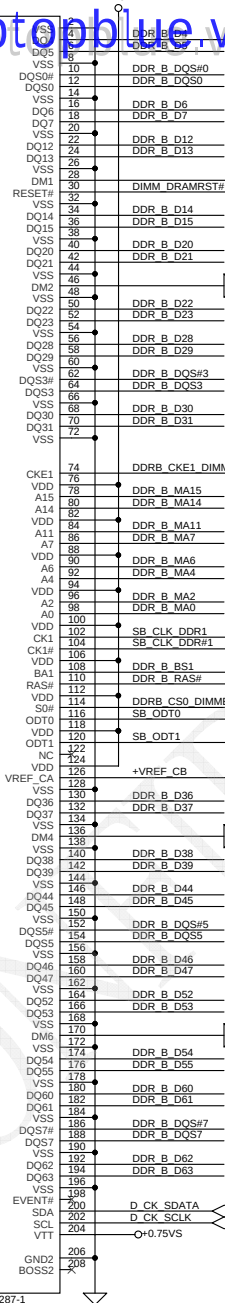
All VREF traces should have 10 mil trace width



<Address: SA1:SA0=10>
12/21 Modify

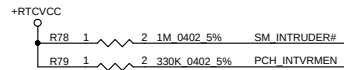
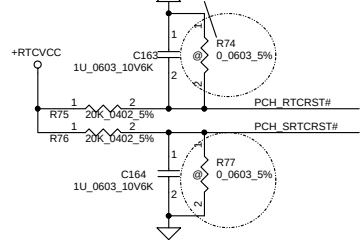
DIMM_2 Reverse H:4.0mm

Channel B

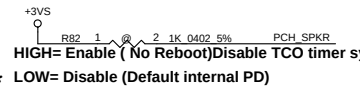


Channel B

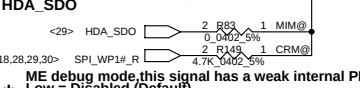
RTCRST close RAM door J1



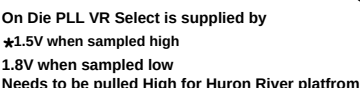
INTRMEN
 ★ H : Integrated VRM enable
 L : Integrated VRM disable
 (INTRMEN should always be pull high.)

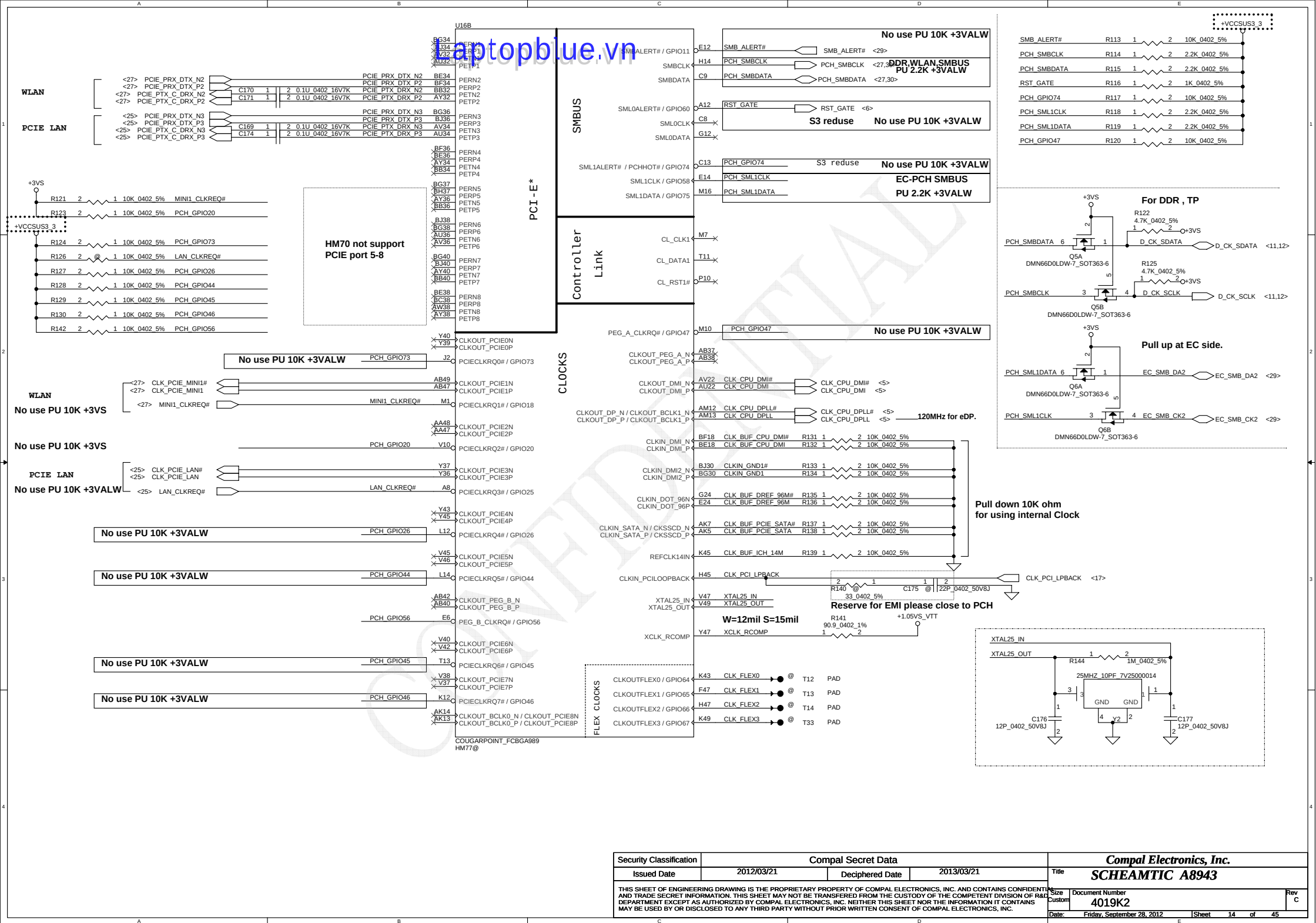


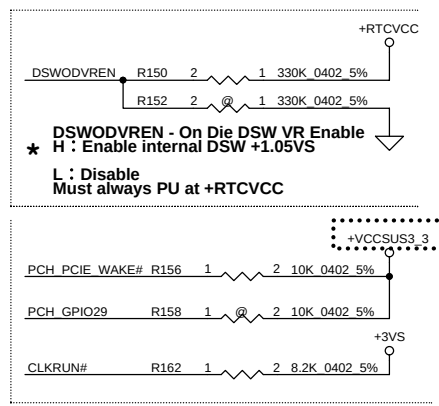
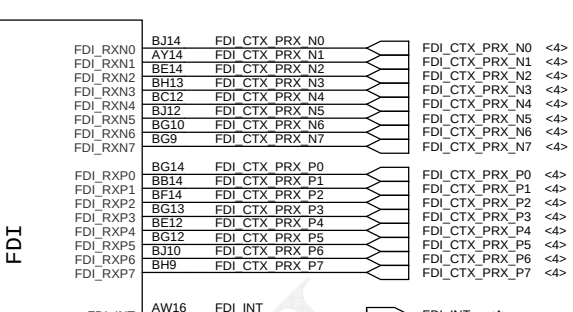
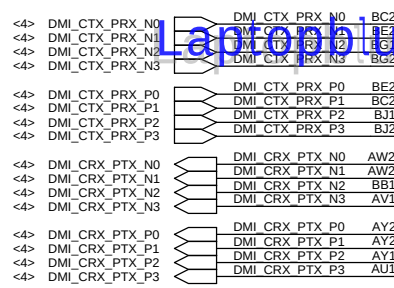
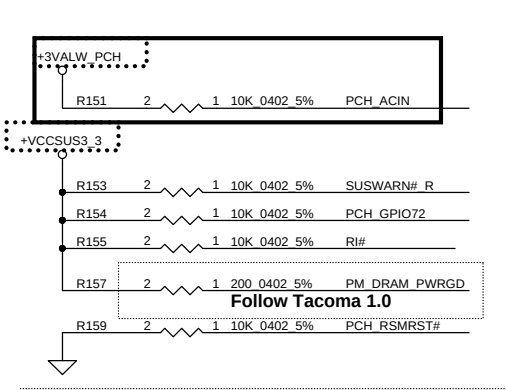
HDA_SDO
 ★ LOW= Disable (Default internal PD)
 ME debug mode this signal has a weak internal PD
 ★ Low = Disabled (Default)
 High = Enabled (Flash Descriptor Security Override)



This signal has a weak internal pull-down
 On Die PLL VR Select is supplied by
 ★1.5V when sampled high
 1.8V when sampled low
 Needs to be pulled High for Huron River platform



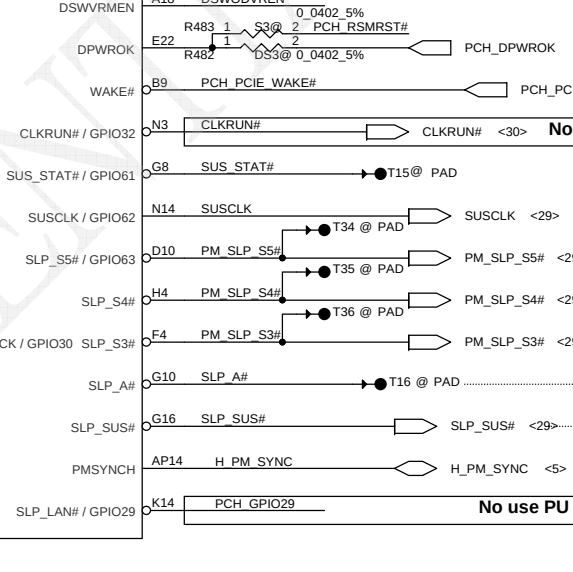
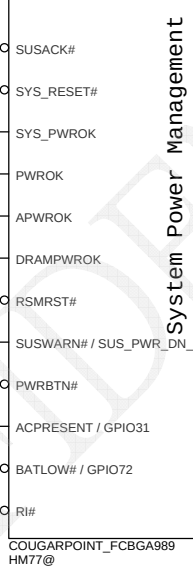
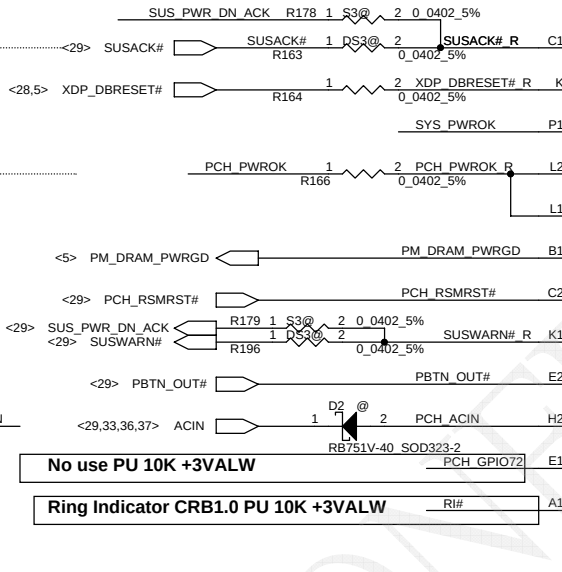
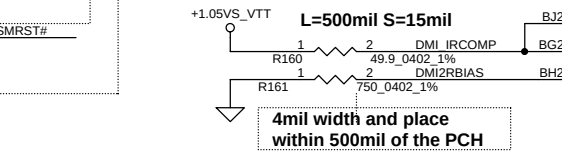
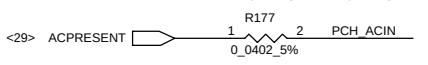




not support Deep S4,S5
can be left unconnected.
Check list1.5 P.81

not support AMT APWROK can mux
with PWROK (check list1.5 P.47)

1/11 Add "ACPRESENT" signal. (follow Q5LJ1)



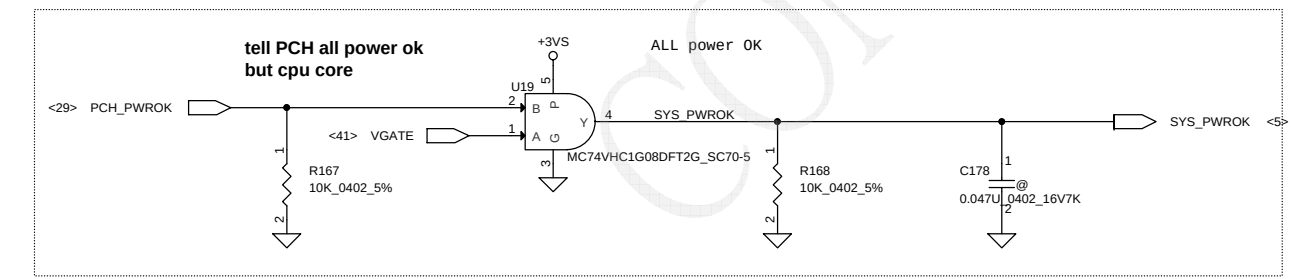
not support Deep S4,S5 DPWROK mux with
RSMRST#
check list1.5 P.50

No use PU 10K +3VS

Can be left NC
when IAMT is not
support on the
platform

not support
Deep S4,S5 can NC
PCH EDS1.5 P.75

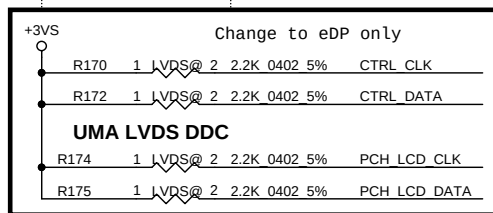
No use PU 10K +3VALW



UMA Panel Backlight ON/OFF

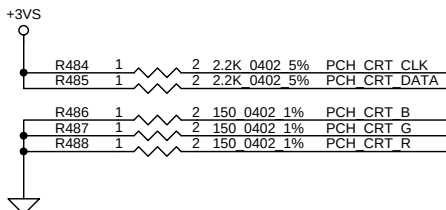
<29> ENBKL ← ENBKL R169 2 1 0 0402 5% IGPU BKLT EN

**PD 100K
at EC side**



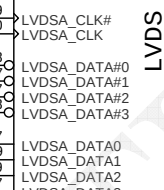
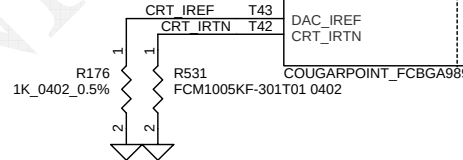
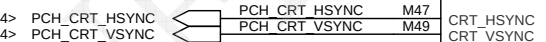
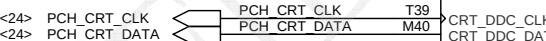
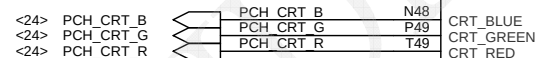
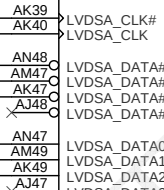
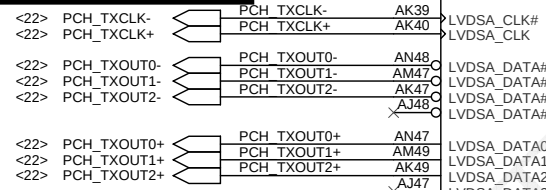
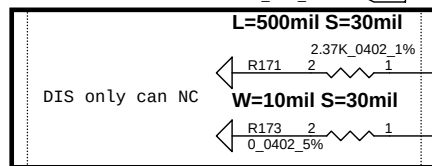
**Check list1.5 P.60 disable Graphics
ALL Can NC
but DAC_IREF still need PD**

**LVDS disable:
DATA/Clock/Control an NC
VCC_TX_LVDS,VCCA_LVDS PD to GND**



**UM77 not support
LVDS/CRT**

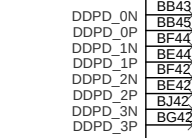
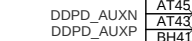
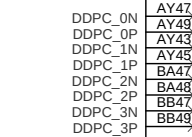
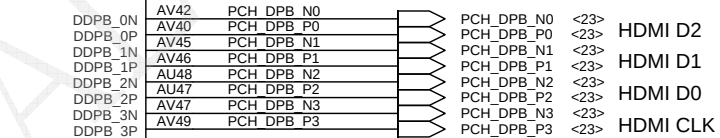
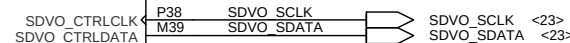
Laptopblue.vn



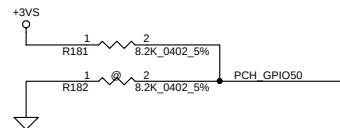
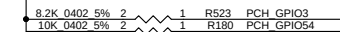
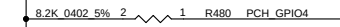
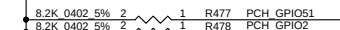
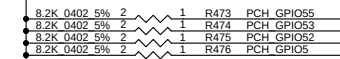
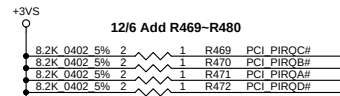
Digital Display Interface



**SDVO_CTRLDATA strap pull high
at level shift page**



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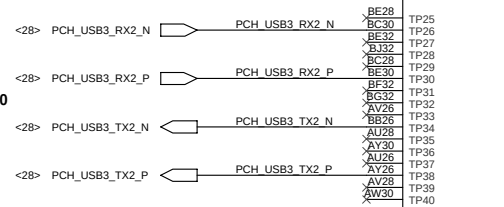
Boot BIOS Strap

GNT1#/ GPIO51	GPIO19 GPIO51 Boot BIOS		Destination
	Bit11	Bit10	
Internal PH	0	1	Reserved
	1	0	PCI
	1	1	SPI *
	0	0	LPC

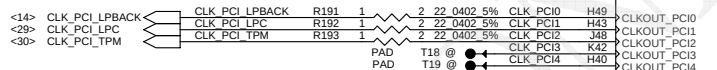
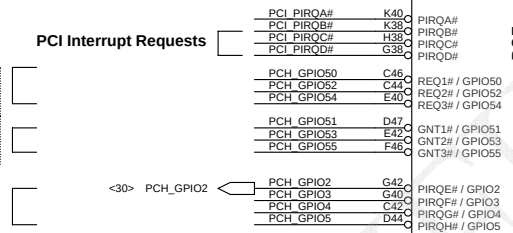
CR Check list 1.5 only use for GPIO
No use PU +3VS

CR Check list 1.5 only use for GPIO
無須PH(Internal PH),如做GPIO PU +3VS

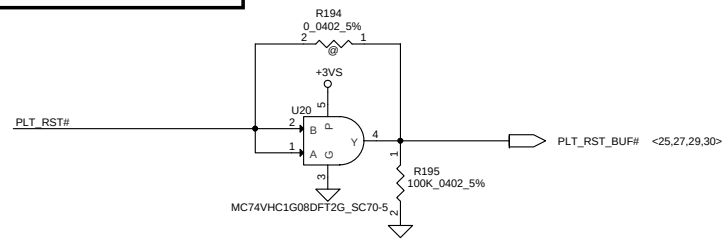
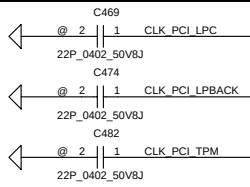
USB3.0



PCI Interrupt Requests



11/30 Add (EMI request)



RSVD

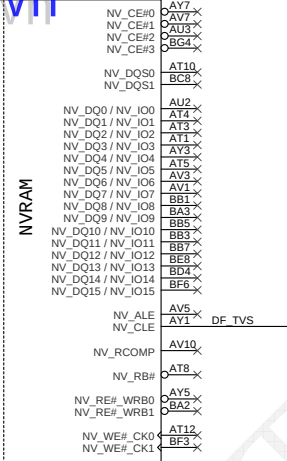
NVRAM

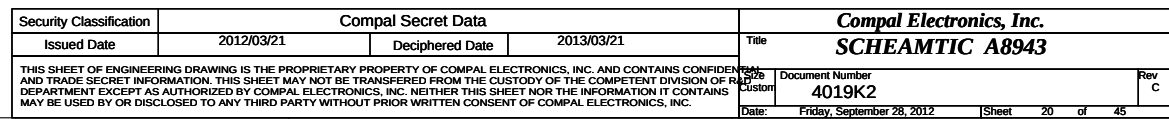
USB

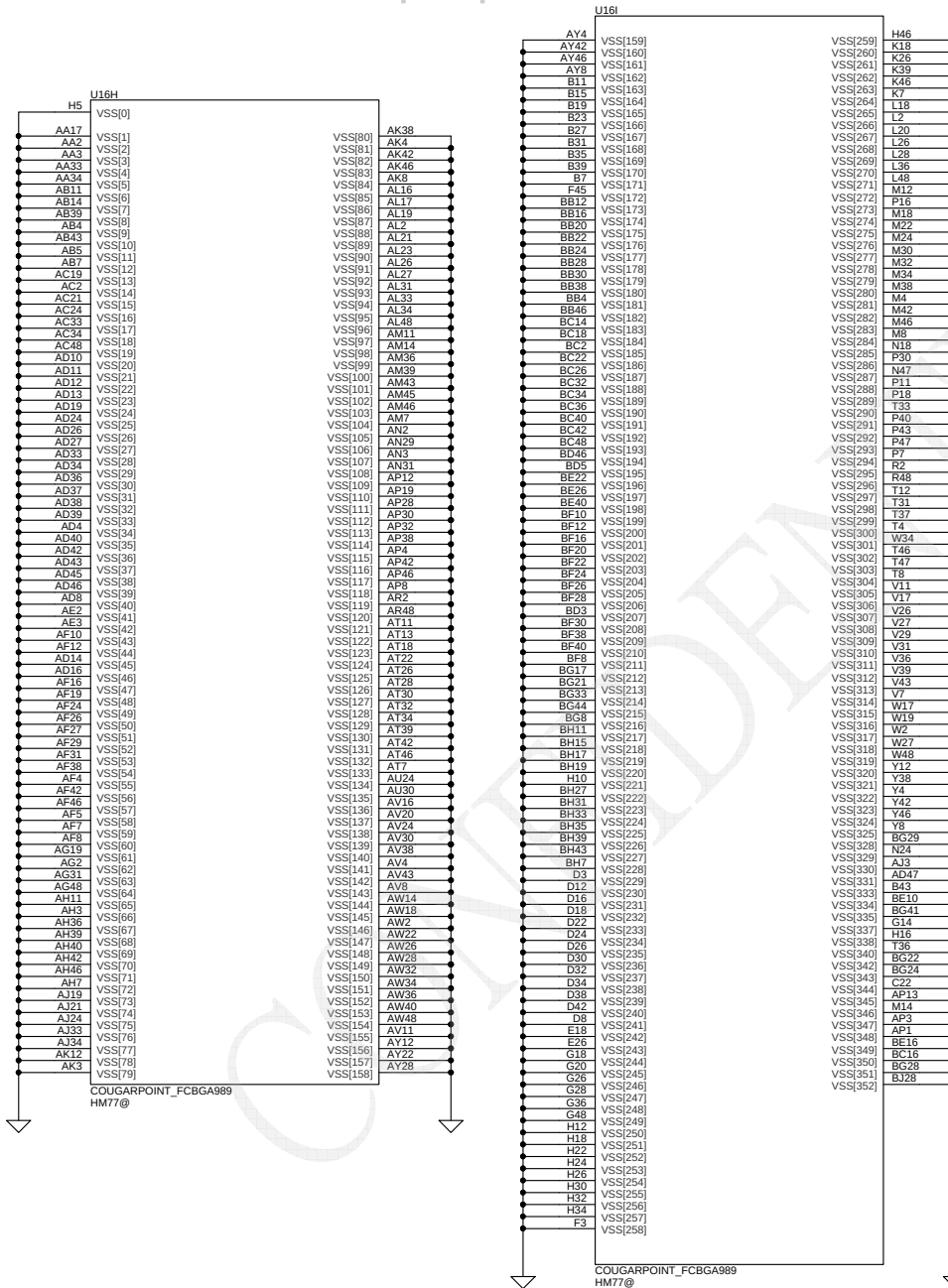
PCI

COUGARPOINT_FCBGA989

HM77@





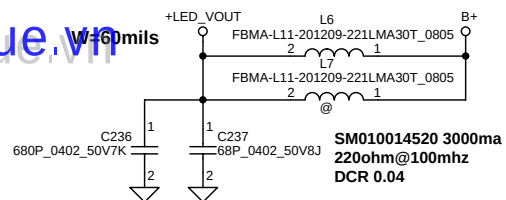
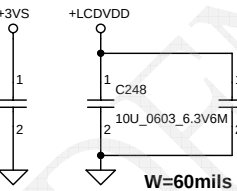
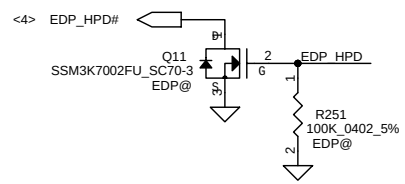
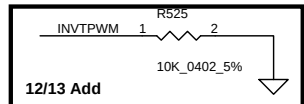
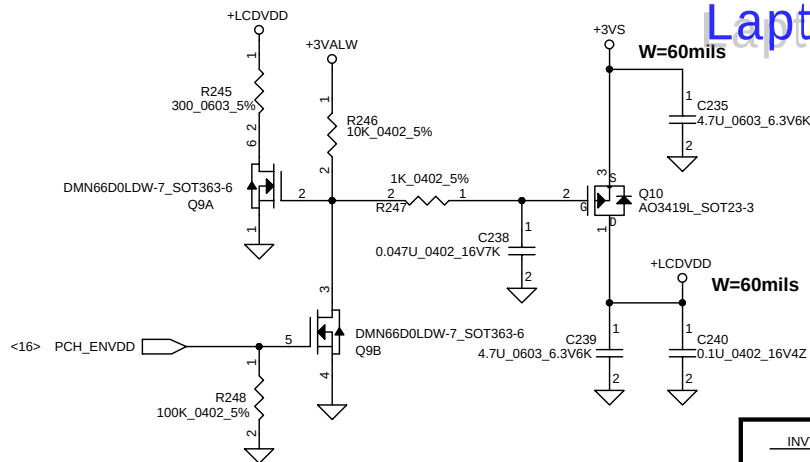


COUGARPOINT_FCBGA989
HM77@

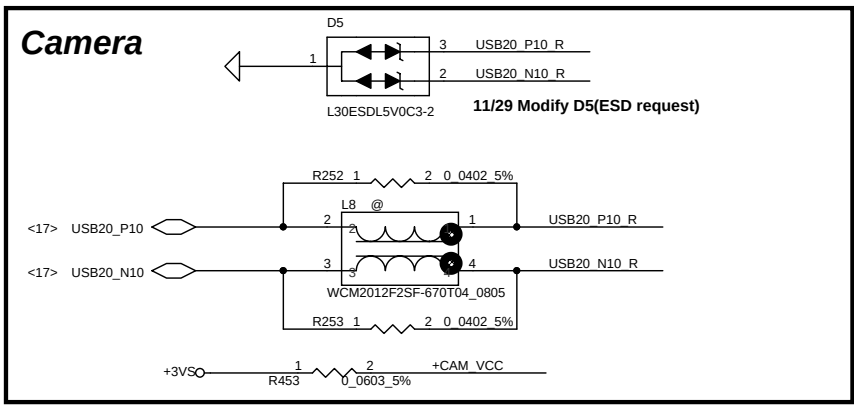
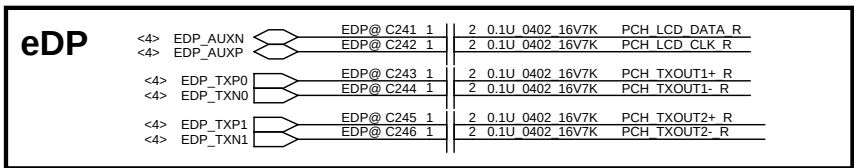
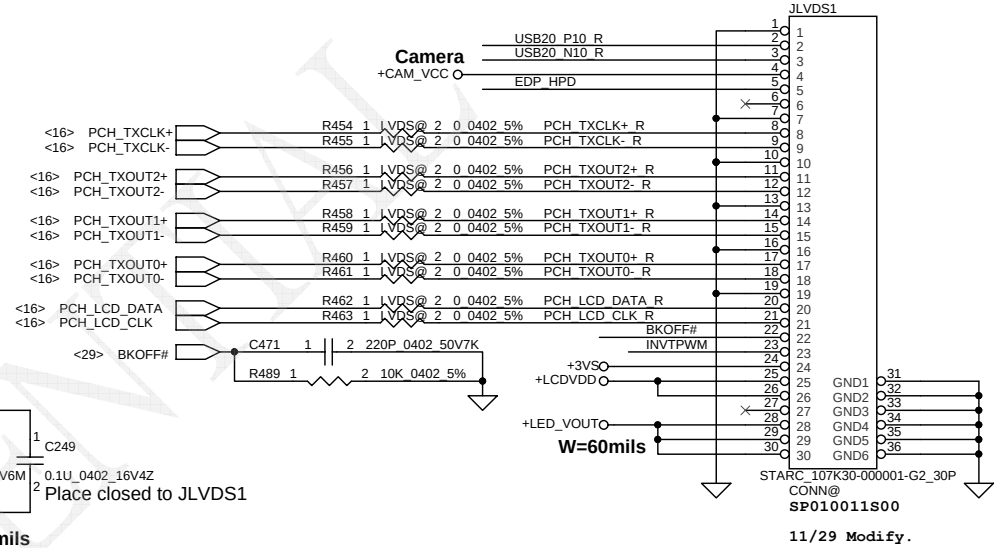
COUGARPOINT_FCBGA989
HM77@

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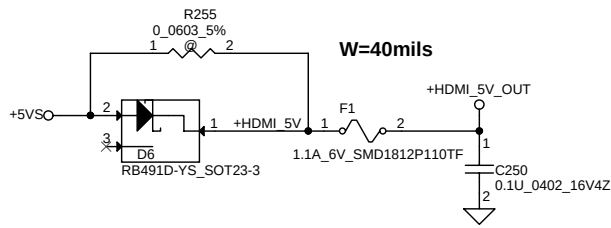
LCD POWER CIRCUIT



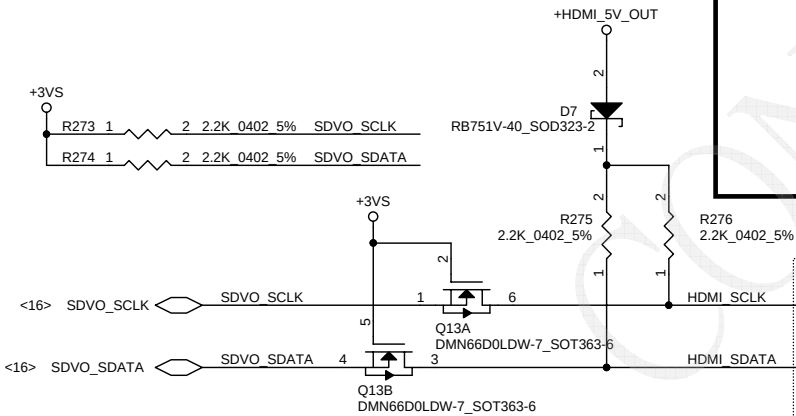
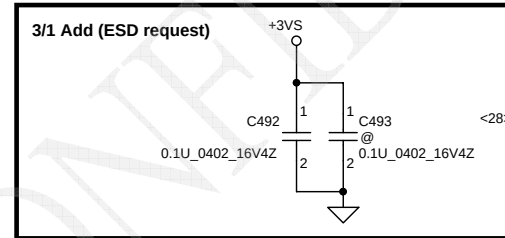
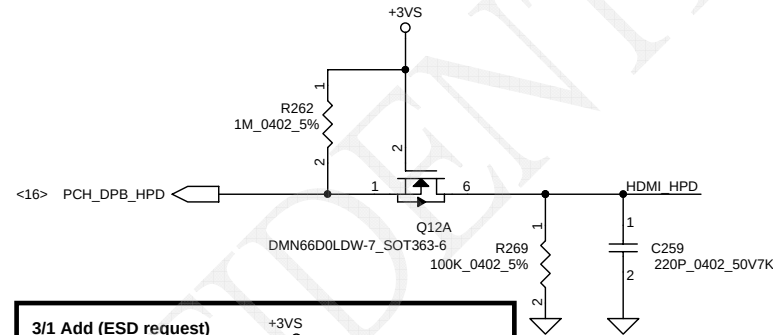
LCD/LED PANEL Conn.



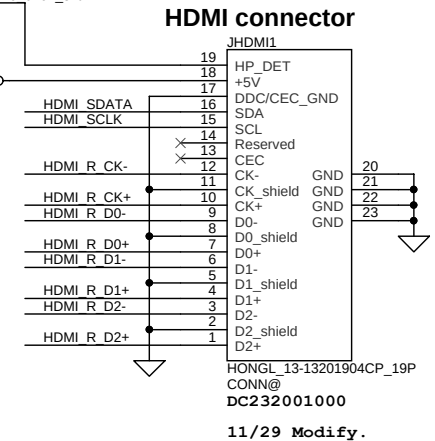
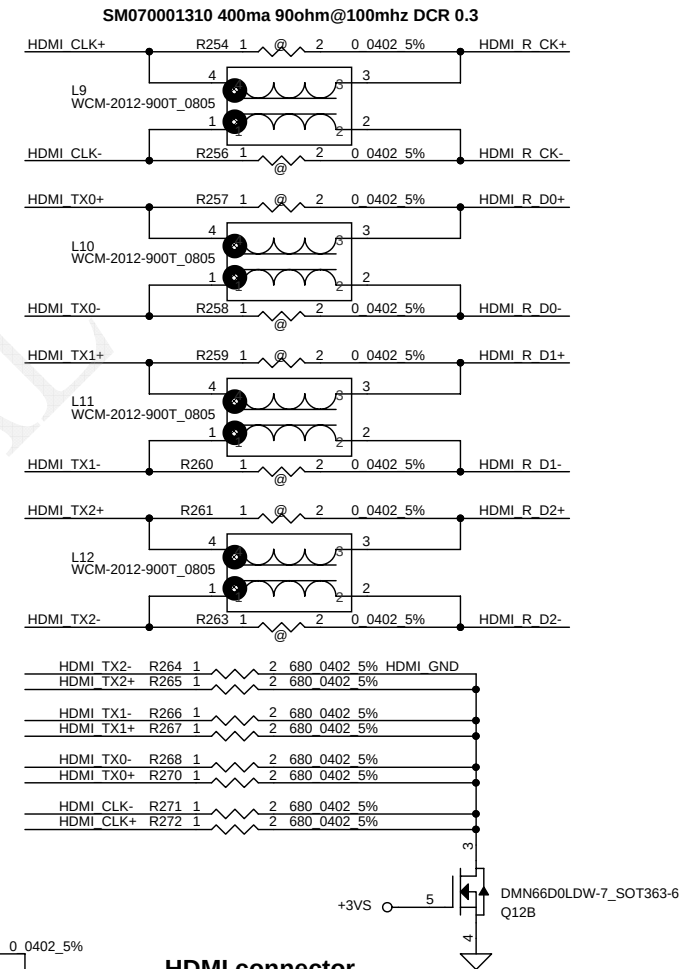
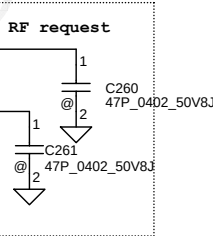
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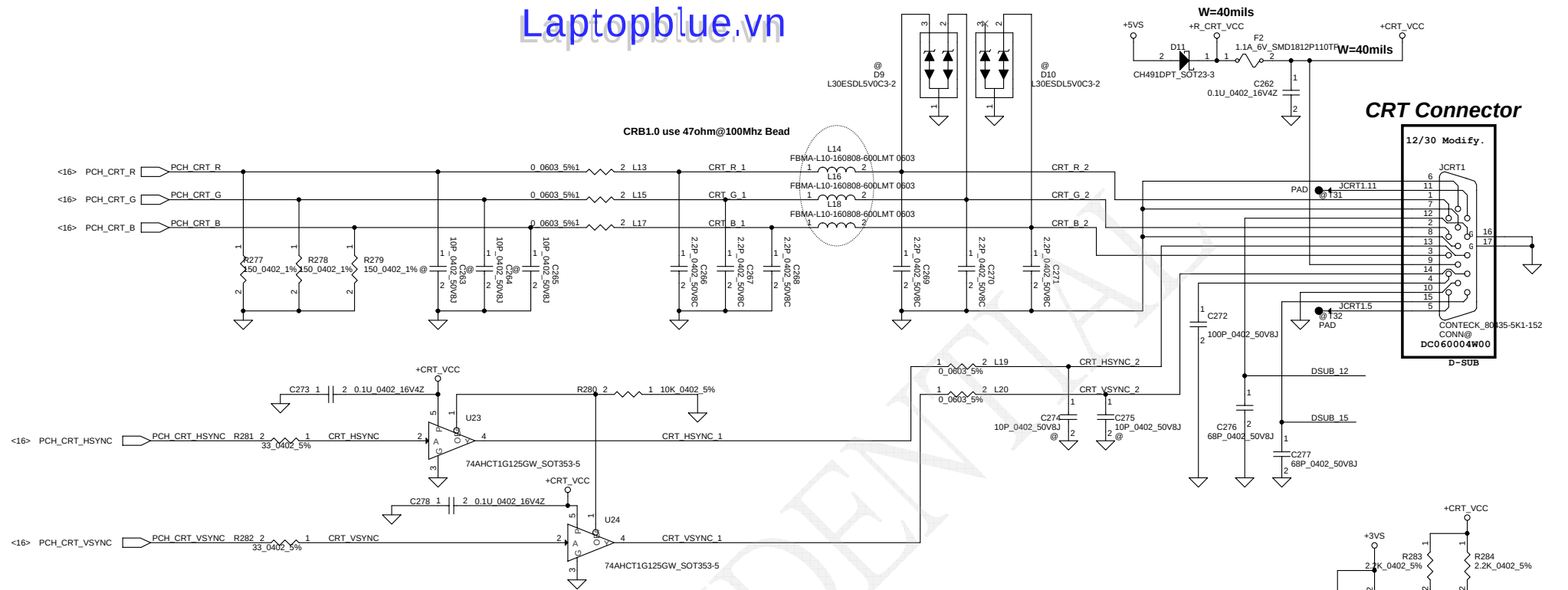
<16>	PCH_DPB_N0	C251	2	1	0.1U_0402_16V7K	HDMI TX2-
<16>	PCH_DPB_P0	C252	2	1	0.1U_0402_16V7K	HDMI TX2+
<16>	PCH_DPB_N1	C253	2	1	0.1U_0402_16V7K	HDMI TX1-
<16>	PCH_DPB_P1	C254	2	1	0.1U_0402_16V7K	HDMI TX1+
<16>	PCH_DPB_N2	C255	2	1	0.1U_0402_16V7K	HDMI TX0-
<16>	PCH_DPB_P2	C256	2	1	0.1U_0402_16V7K	HDMI TX0+
<16>	PCH_DPB_N3	C257	2	1	0.1U_0402_16V7K	HDMI CLK-
<16>	PCH_DPB_P3	C258	2	1	0.1U_0402_16V7K	HDMI CLK+



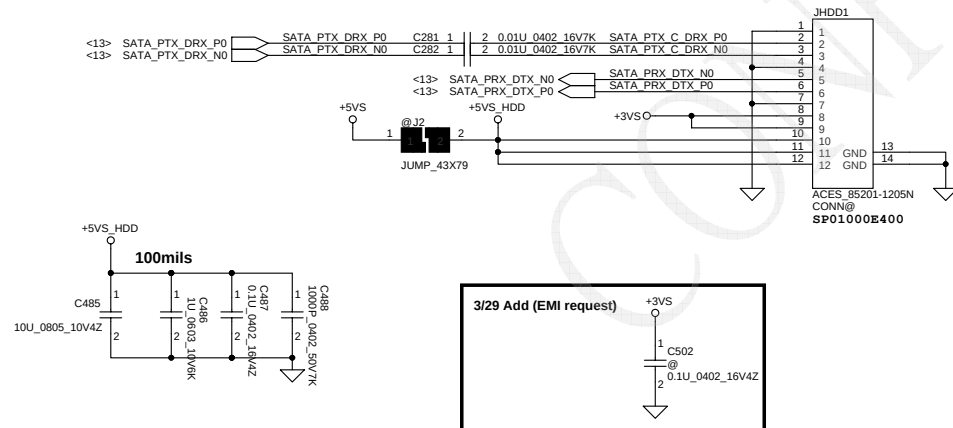
Place closed to JHDMI1



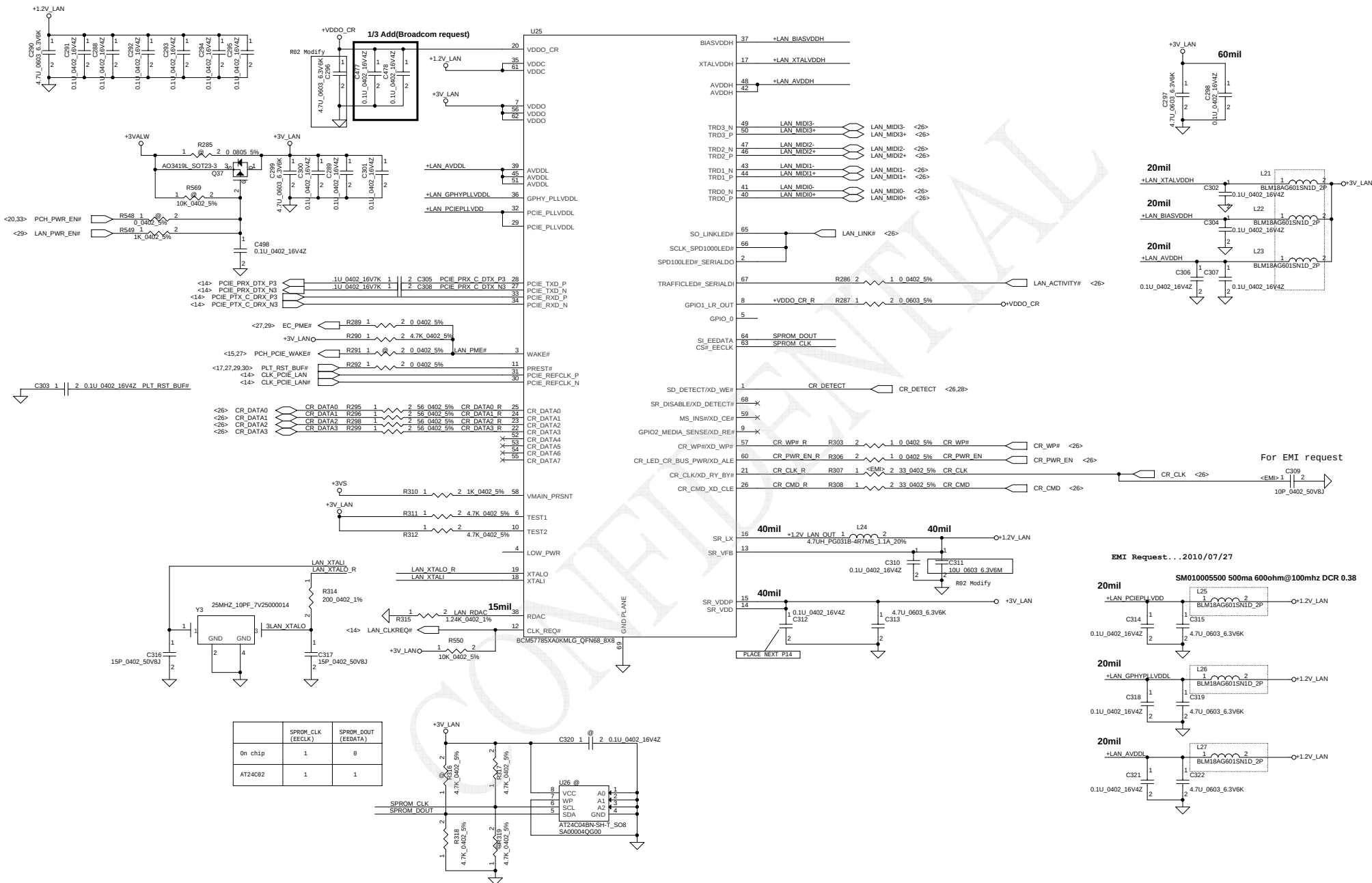
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HDD Board Conn



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C474,C475 and D14
ME interfere,do not pop!!

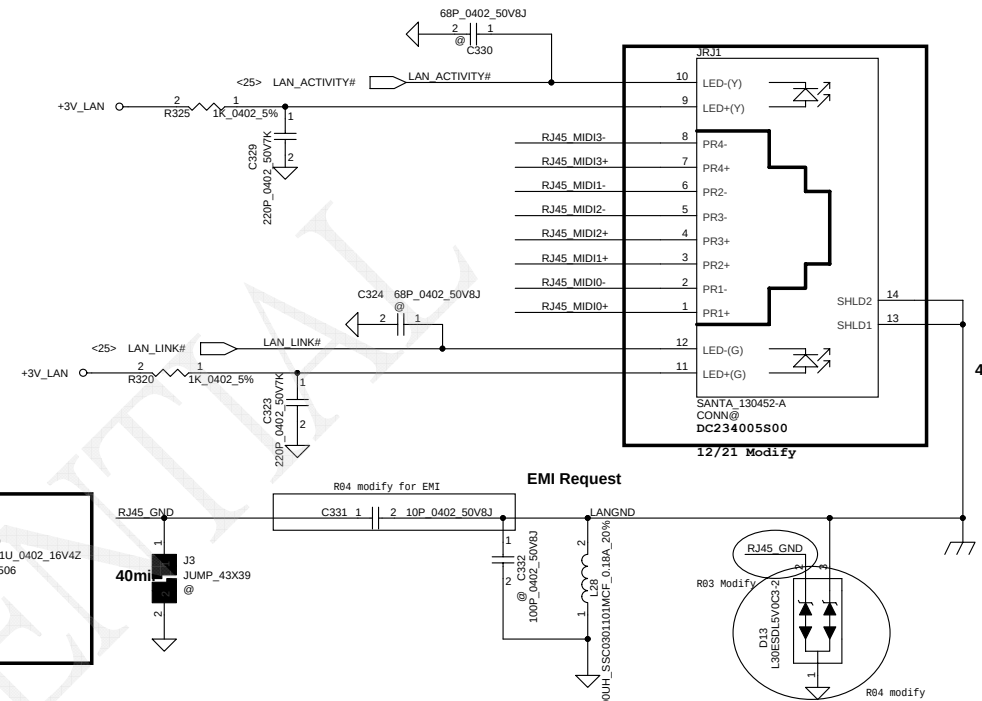
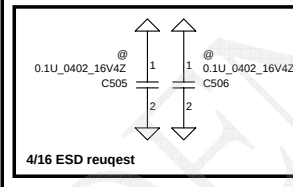
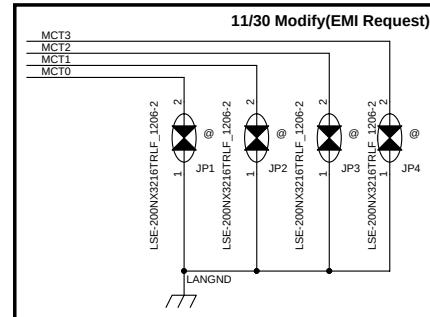
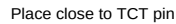


Diagram illustrating the connection of the SP07000TF00 12/23 Modify (2in1 CARD READER) to the JREAD1 header.

Signal Connections:

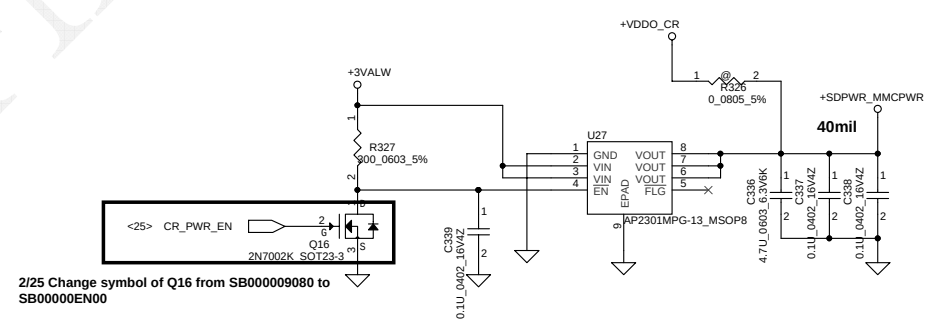
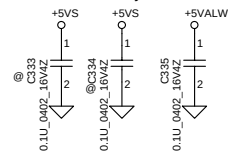
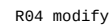
- CR_CMD:** Connected to JREAD1 pin 3. Signal source: <25> CR_CMD.
- CR_CLK:** Connected to JREAD1 pin 5. Signal source: <25> CR_CLK. A resistor R570 (2) is connected between the signal source and the header.
- CR_DATA0:** Connected to JREAD1 pin 8. Signal source: <25> CR_DATA0.
- CR_DATA1:** Connected to JREAD1 pin 9. Signal source: <25> CR_DATA1.
- CR_DATA2:** Connected to JREAD1 pin 1. Signal source: <25> CR_DATA2.
- CR_DATA3:** Connected to JREAD1 pin 2. Signal source: <25> CR_DATA3.
- CR_WP#:** Connected to JREAD1 pin 10. Signal source: <25> CR_WP#.
- CR_DETECT:** Connected to JREAD1 pin 11. Signal source: <25,28> CR_DETECT. A resistor R501 (2) is connected between the signal source and the header.

Power and Ground Connections:

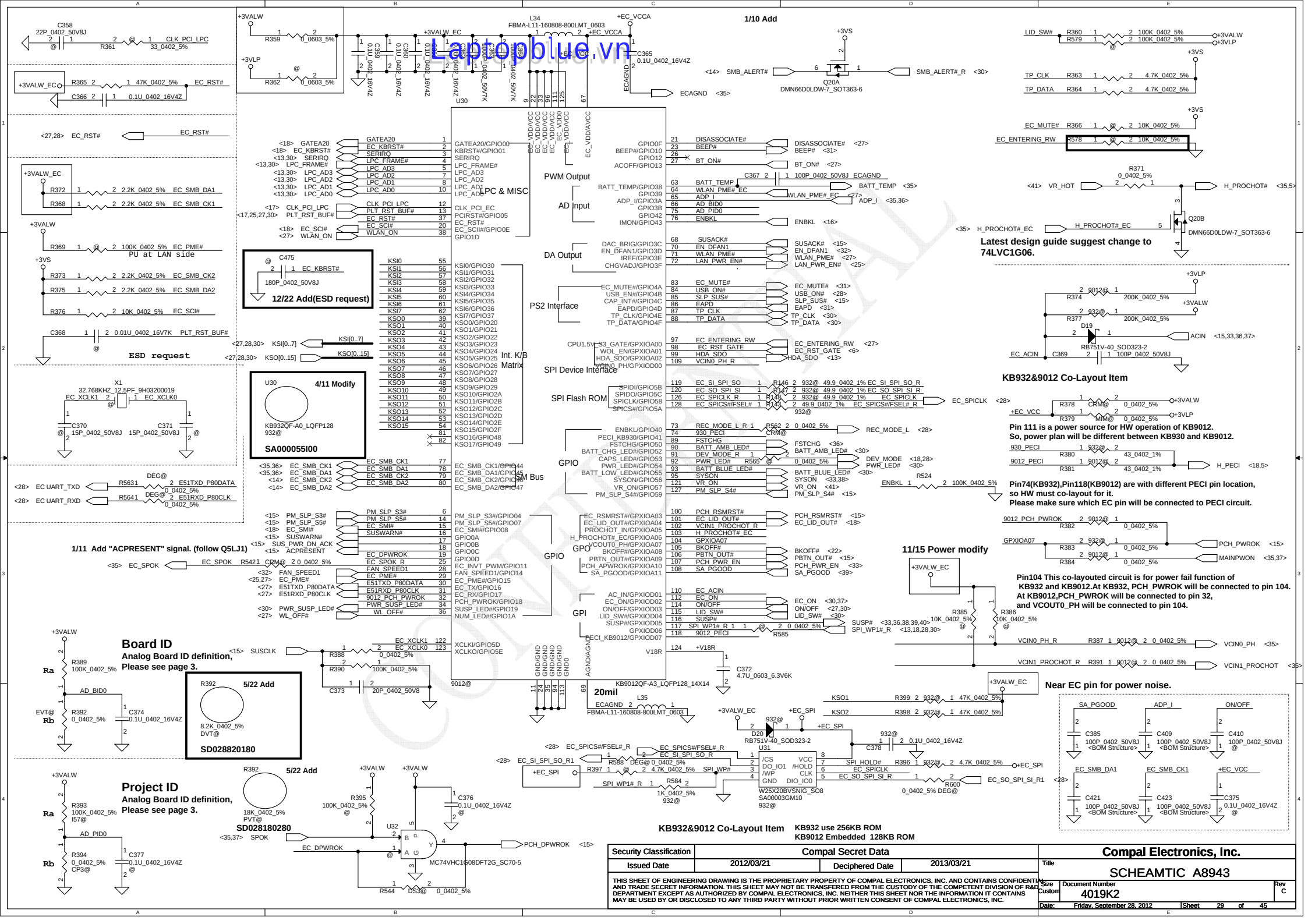
- VSS:** Connected to JREAD1 pins 4 and 7.
- VDD:** Connected to JREAD1 pin 6.
- CLK:** Connected to JREAD1 pin 8.
- WP SW:** Connected to JREAD1 pin 10.
- CD SW:** Connected to JREAD1 pin 11.
- GND SW:** Connected to JREAD1 pin 12.
- GND:** Connected to JREAD1 pins 14 and 15.

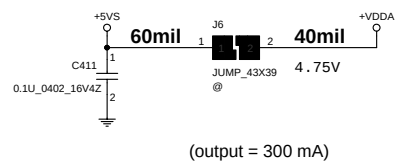
Notes:

- CONN@
- 1.SOL_156-1000302601_11P
- SP07000TF00
- 12/23 Modify (2in1 CARD READER)
- (板上2.85mm)

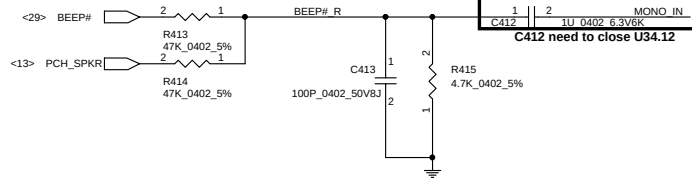


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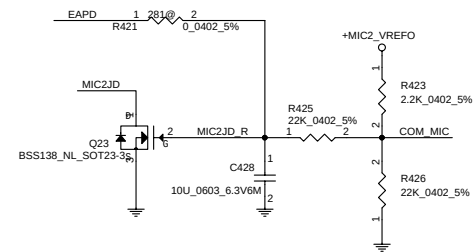
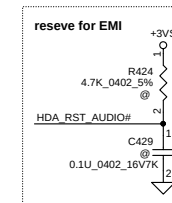
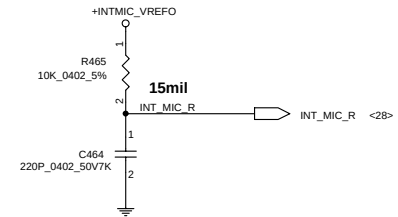
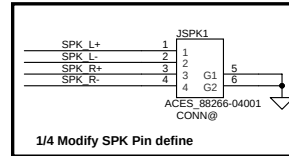
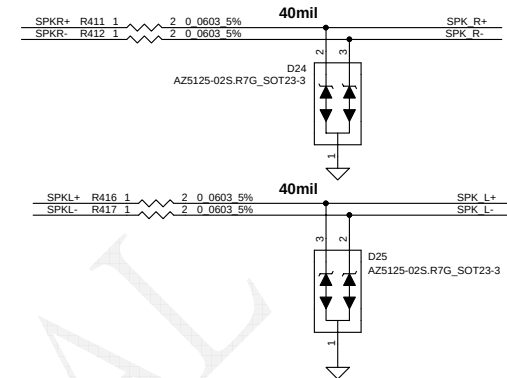
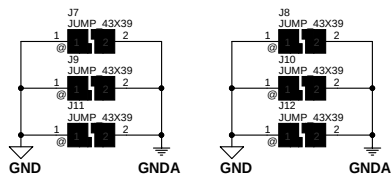
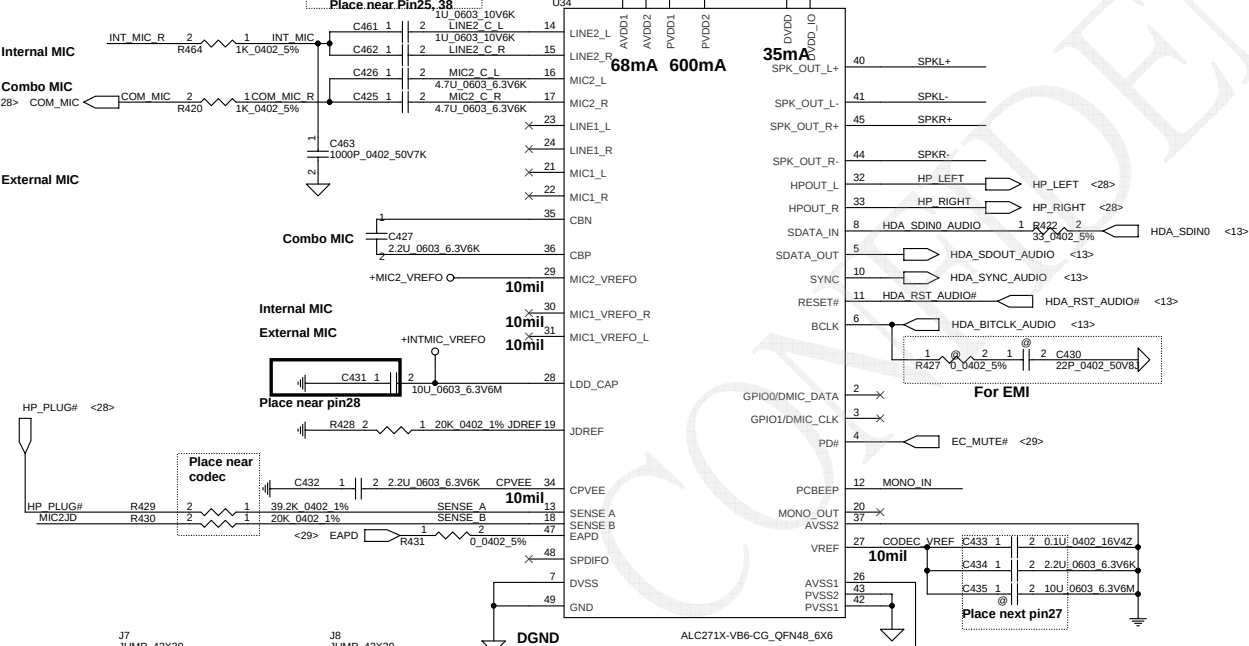
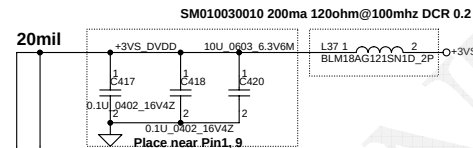
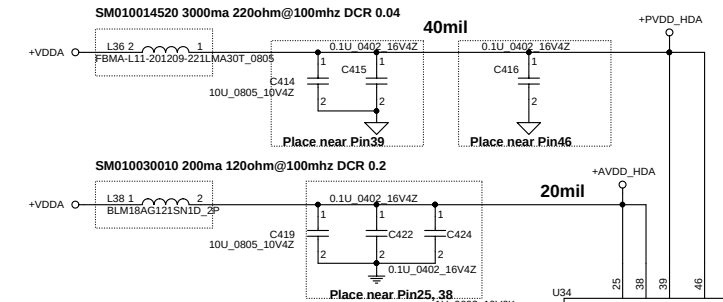




(output = 300 mA)



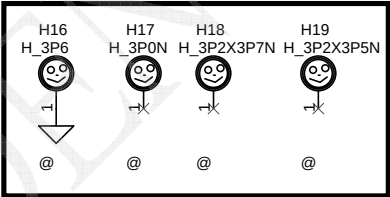
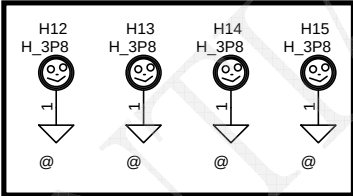
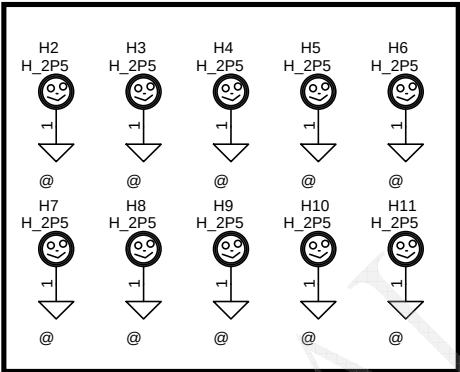
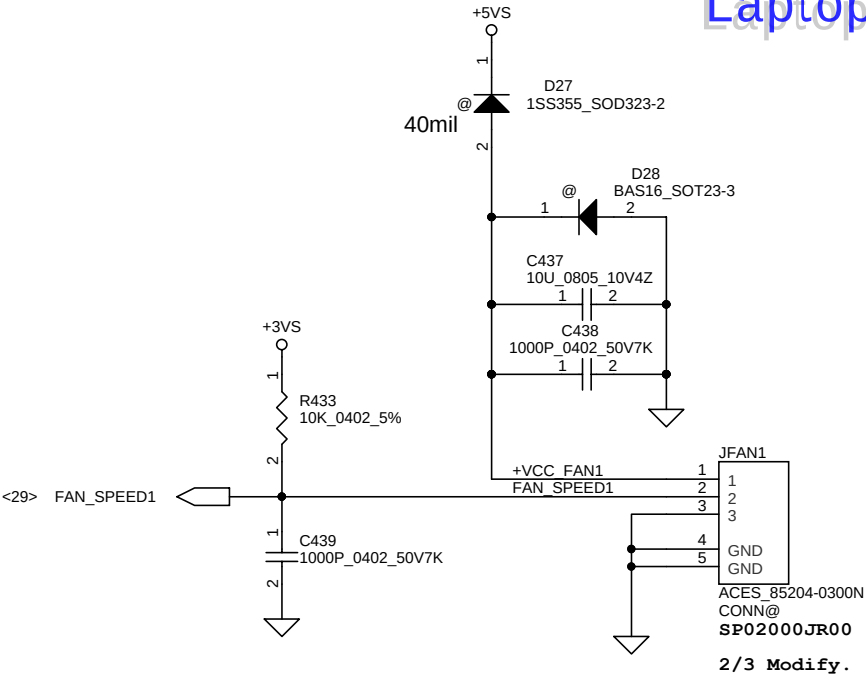
HD Audio Codec



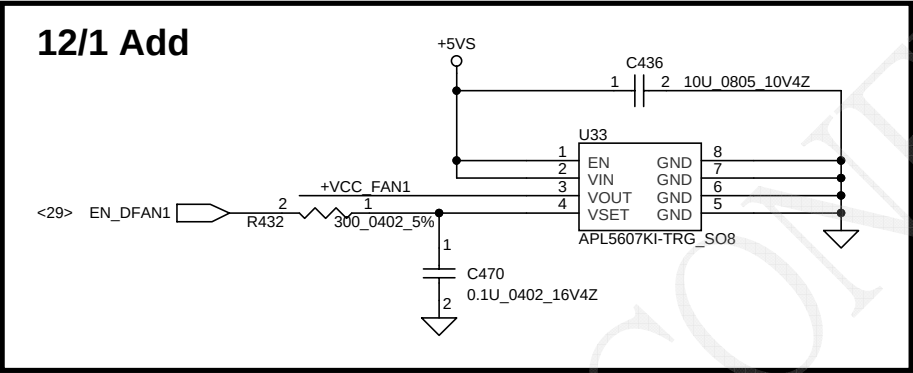
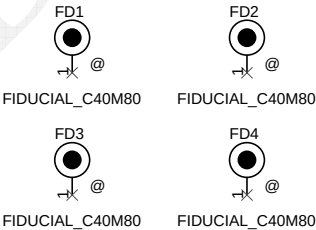
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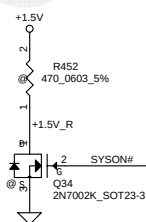
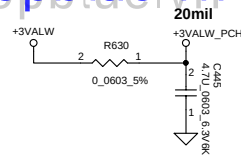


CPU support plate

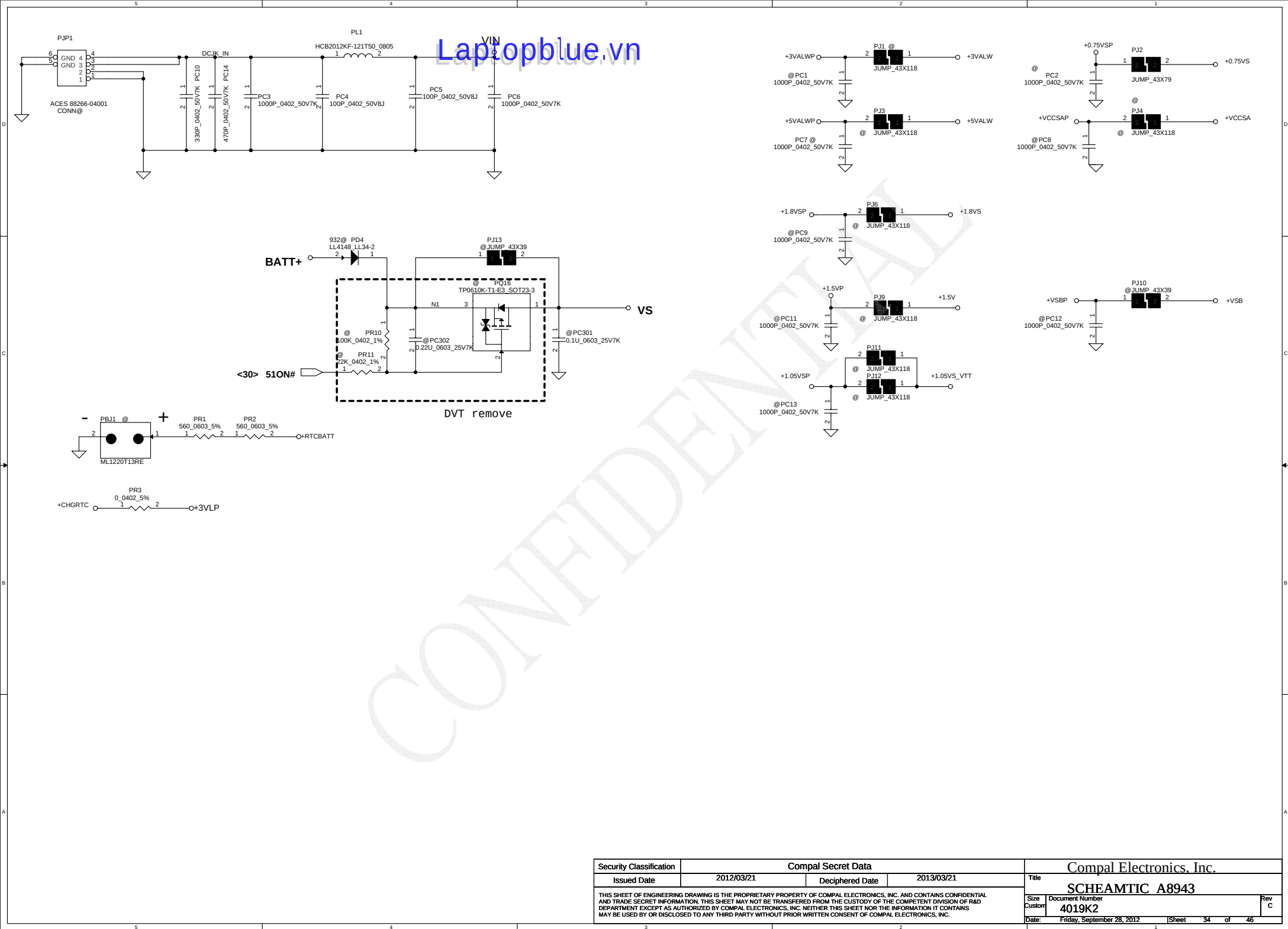


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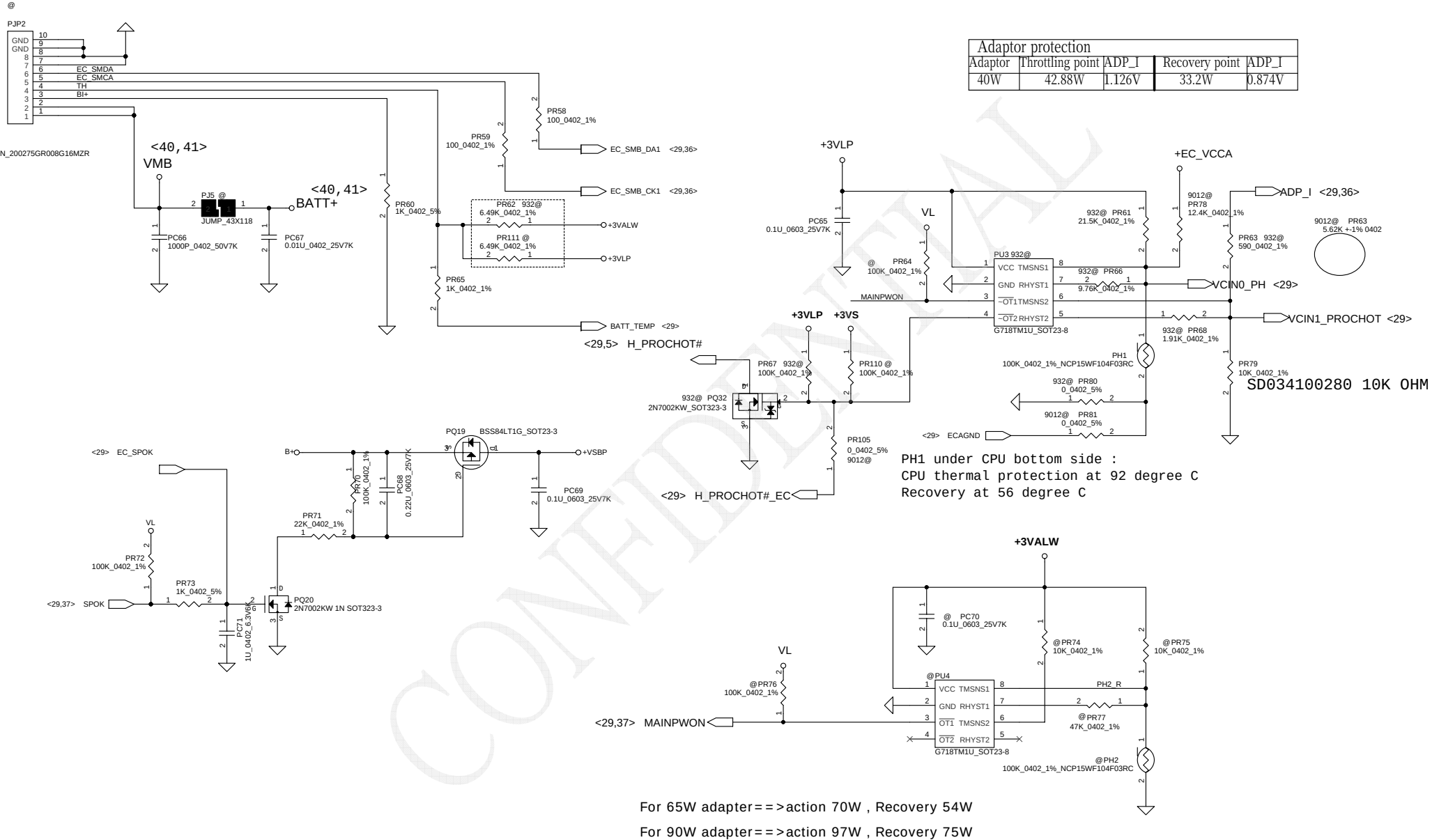
+3VALW to +3VALW_PCH(PCH AUX Power)



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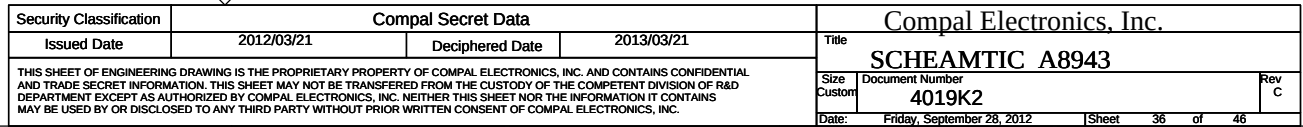
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PN:DC040007N10 SOCKET BATT C200275MR008G15QZR 8P W/FORK

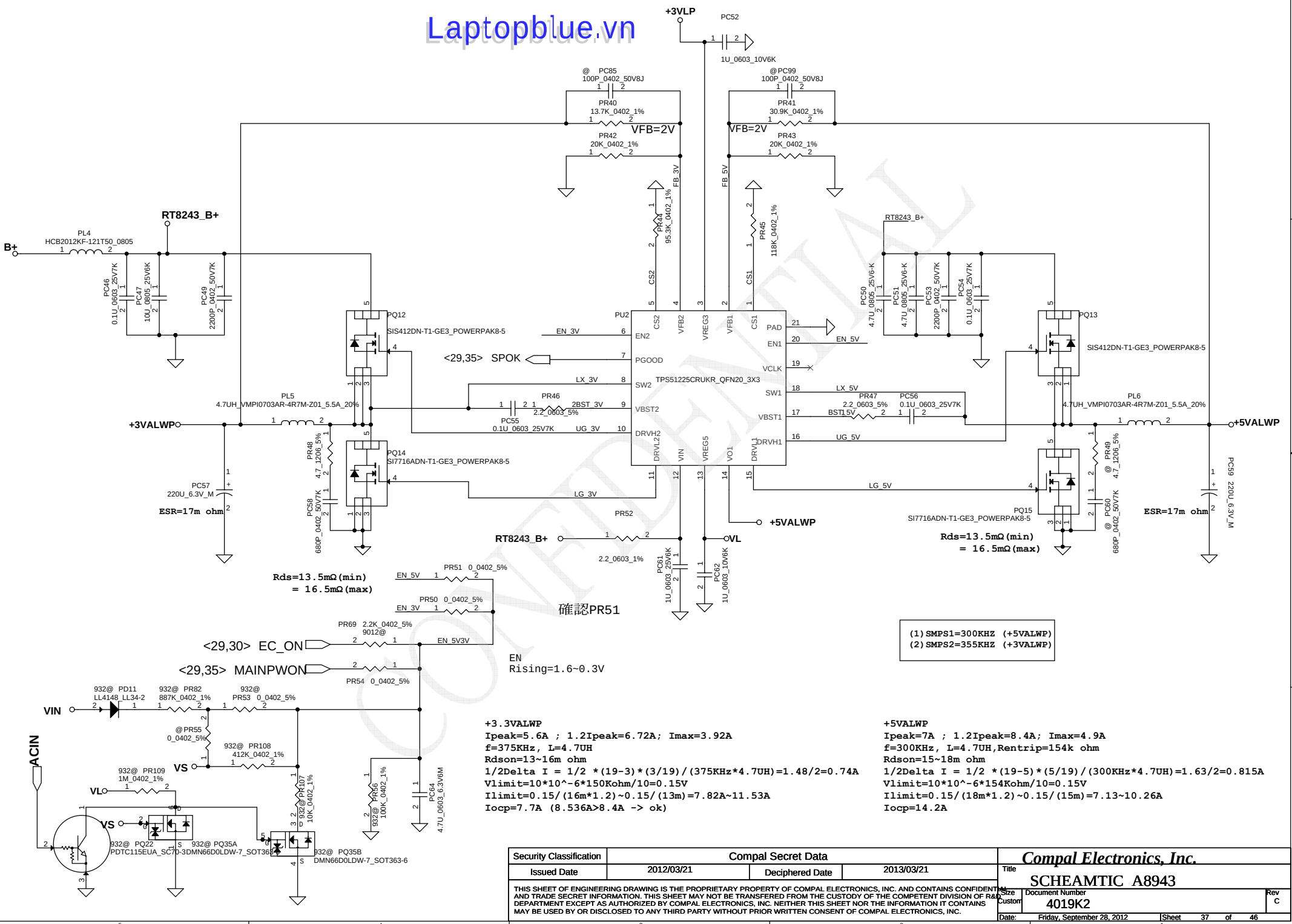


For 65W adapter==>action 70W , Recovery 54W
For 90W adapter==>action 97W , Recovery 75W

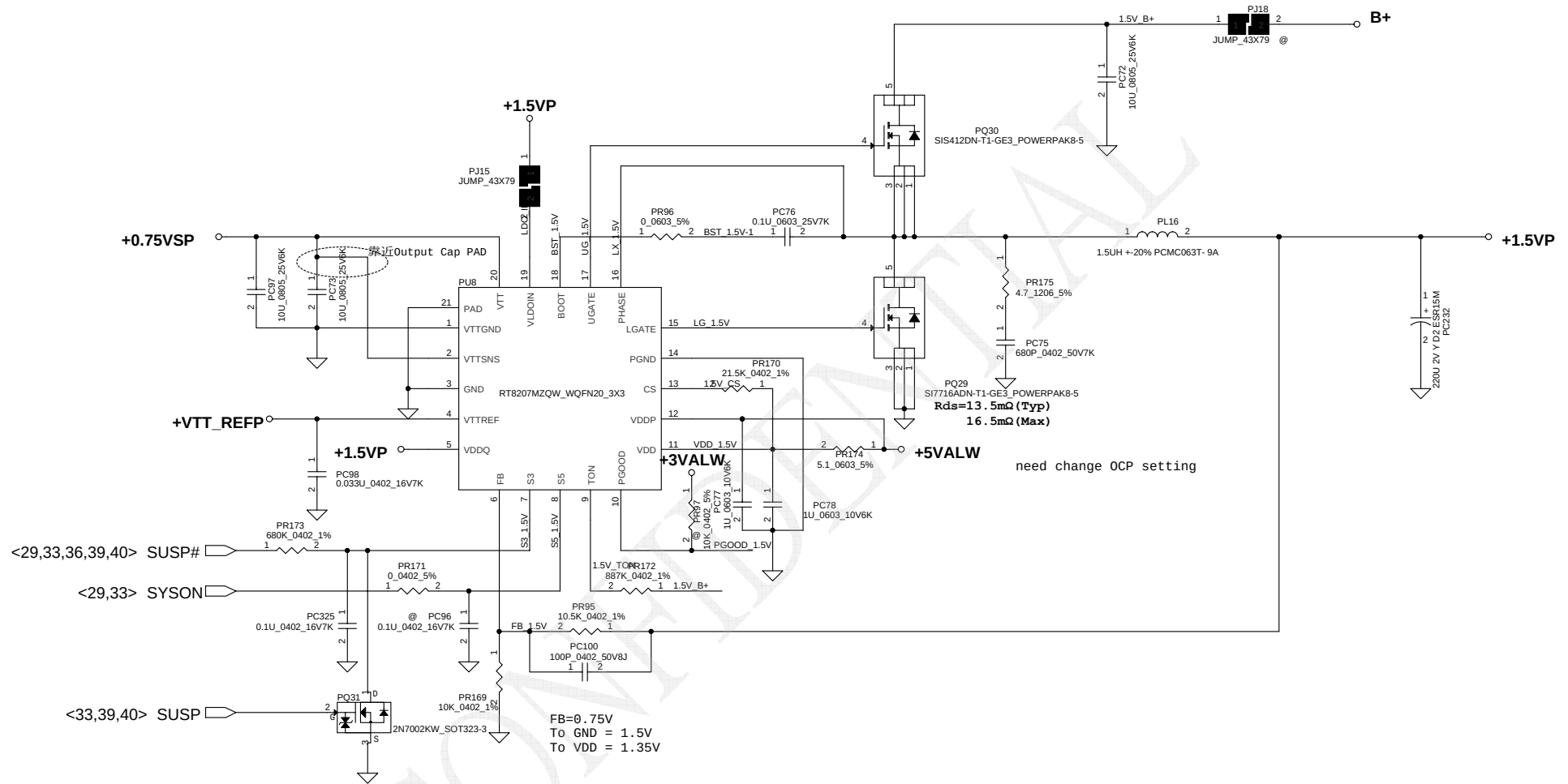
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STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

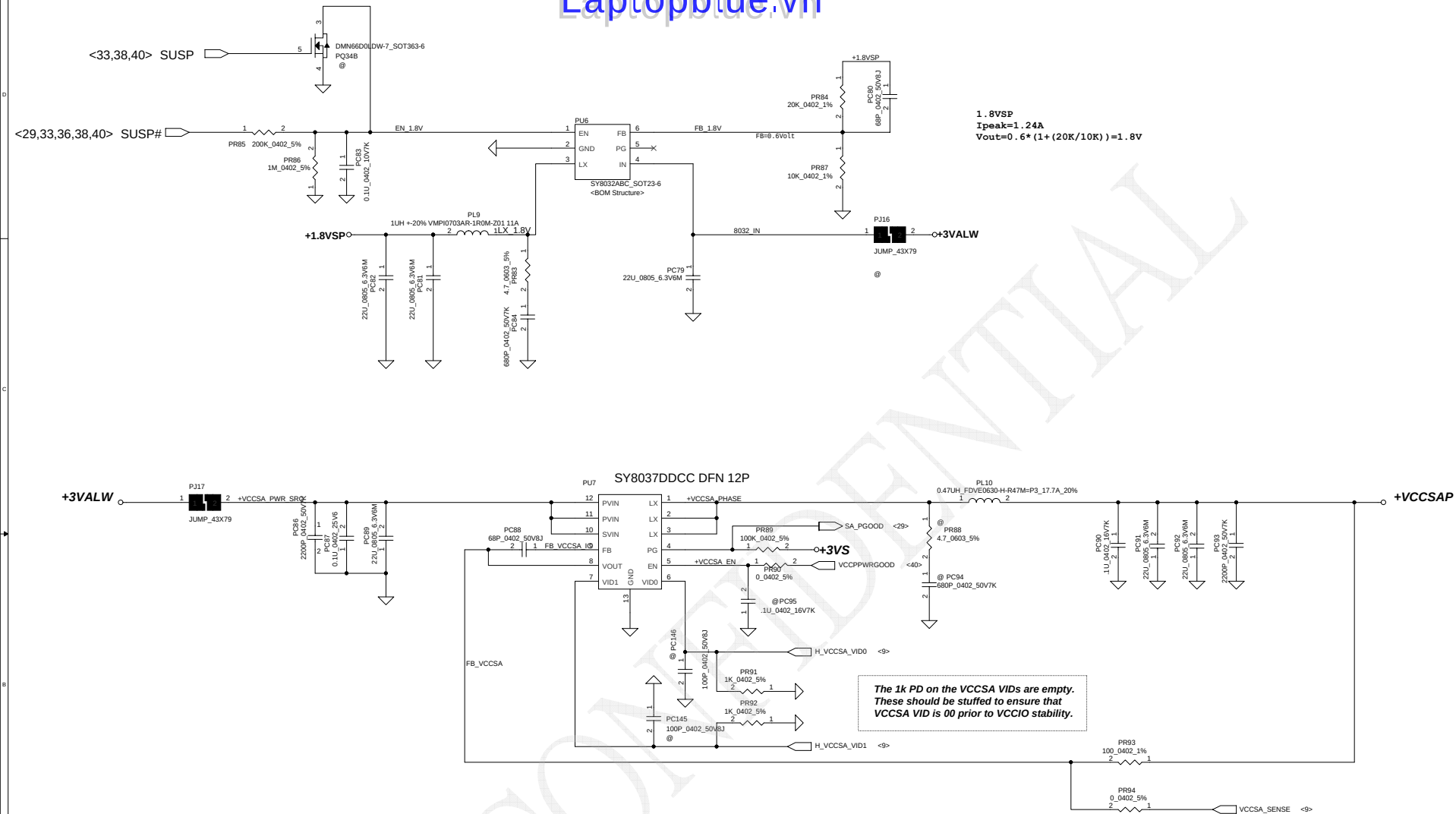
Note: S3 - sleep ; S5 - power off

<Vo=1.5V> VFB=0.75V
 $V = 0.75 * (1 + 10K / 10.5K) = 1.52V$
 $F_{sw} = 286K$ to 200KHz

Cout ESR=17m ohm Rdson(max)=16.5 mohm Rdson(typ)=13.5 mohm.
 $I_{peak} = 12A$, $I_{max} = 8.4A$, $I_{ocp} = 14.4A$

$\Delta I = ((V_{in} - V_o) * (V_o / V_{in})) / (L * F_{sw}) = 2.195A$
 $\Rightarrow 1/2 \Delta I = 1.099A$

$I_{ocpmax} = ((21.5K * 11uA) / 0.0135) + 0.5 \Delta I = A$
 $I_{ocpmin} = ((21.5K * 9uA) / (0.0165)) + 0.5 \Delta I = 15.6A$



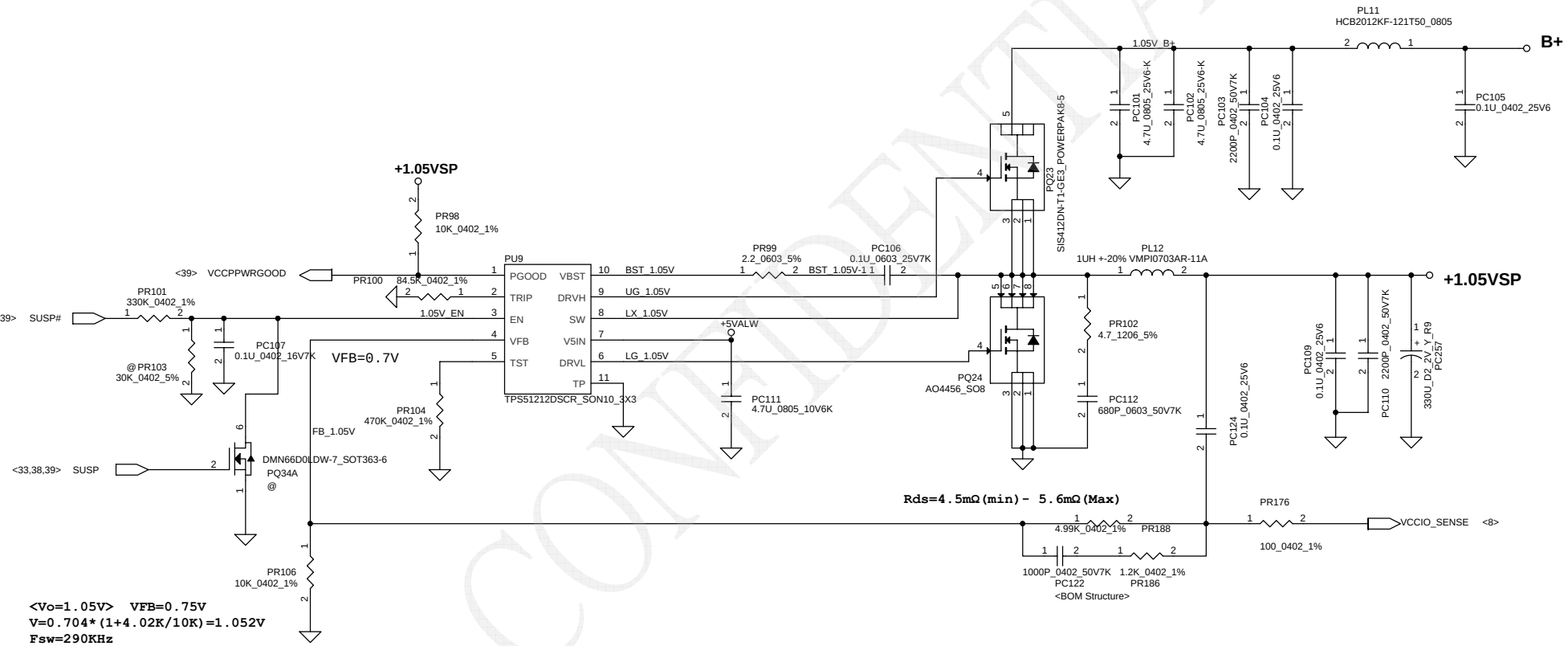
1.8VSP
Ipeak=1.24A
Vout=0.6*(1+(20K/10K))=1.8V

The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.

+VCC SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

VID [0]	VID[1]	VCCSA Vout (uV only)
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network

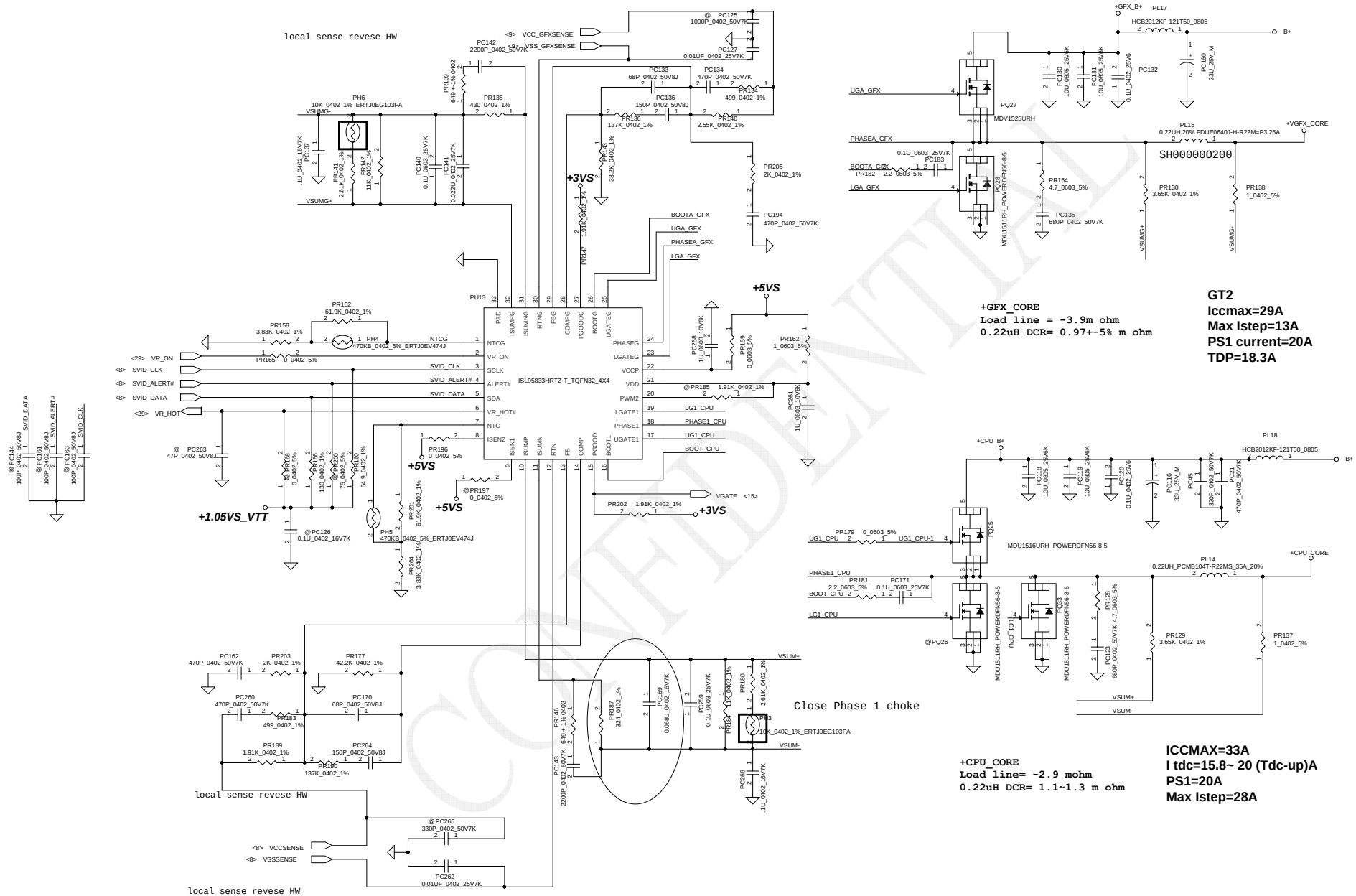


Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=15.6A, Imax=10.92A, Iocp=18.72A

Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=2.06A

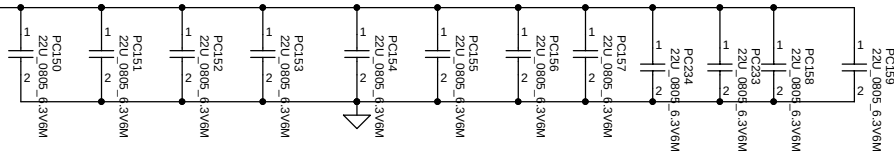
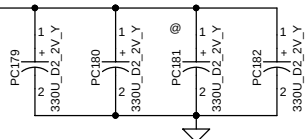
Iocpmax=((15K*11uA)/0.0045)+1.665A=23.54A
Iocpmin=((15K*9uA)/(0.0056*1.3))+1.665A=19A
Iocp=A

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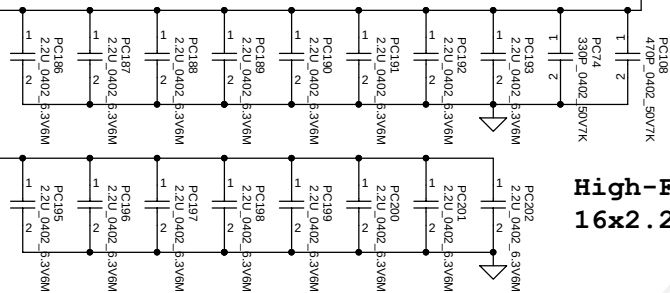
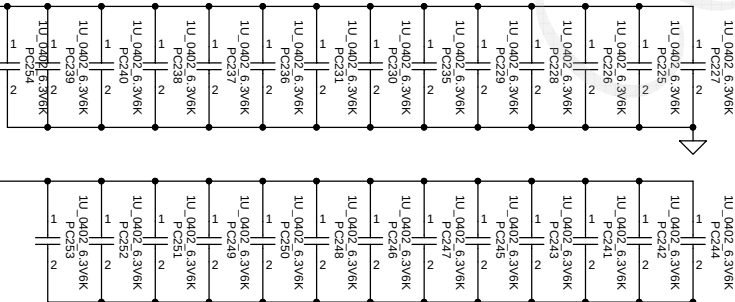
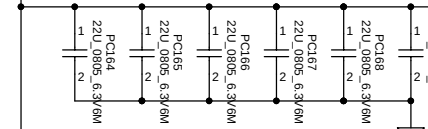
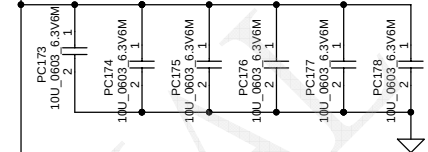
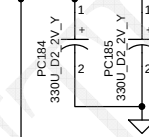
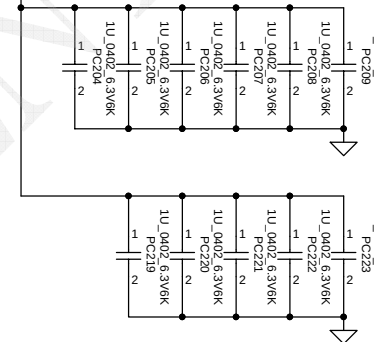
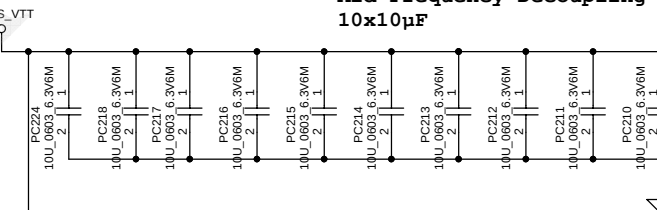


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CR PDDG Rev 0.95

Mid-Frequency Decoupling
12x22 μ F**Low-Frequency Decoupling**
3x330 μ F 9m

+CPU_CORE

High-Frequency Decoupling
16x2.2 μ F**High-Frequency Decoupling**
27x1 μ F**Mid-Frequency Decoupling**
6x22 μ F**Mid-Frequency Decoupling**
6x10 μ F 0603**Low-Frequency Decoupling**
2x330 μ F 9m**High-Frequency Decoupling**
11x1 μ F**Mid-Frequency Decoupling**
10x10 μ F**Low-Frequency Decoupling**
1x330 μ F 9m

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Modify DCIN/Pre-change power circuit	0.1	34	Add PC301 330P_0402_50V7K, PC302 470P_0402_50V7K for EMI solution	2012/4/5	EVT
2		Modify Battery CONN/OTP power circuit	0.1	35	Add PR80 0ohm to GND for BOM control (9012 AGND)	2012/4/5	EVT
3		Modify CHARGER	0.1	36	Add PC16,PC63 330P_0402_50V7K, PC20, PC48 470P_0402_50V7K, PC113, PC114, PC115, PC117, PC121 0.1U_0402_25V6 PR26 4.7_1206_5%, PC39 680P_0402_50V7K for EMI solution	2012/4/5	EVT
4		Modify 3VALWP/5VALWP power circuit	0.1	37	Add Snubber PR48 4.7_1206_5%, PC58 680P_0402_50V7K for EMI solution	2012/4/5	EVT
5		Modify 1.5VP/0.75VSP power circuit	0.1	38	Add Snubber PR175 4.7_1206_5%, PC75 680P_0402_50V7K for EMI solution	2012/4/5	EVT
6		Modify 1.05VS power circuit	0.1	40	Delete PR105 5.1K_0402_1%; PR178 0_0402_5%, Add PR188 4.99K_0402_1%; PR186 1.2K_0402_1%, PC122 1000P_0402_50V7K; PC124 0.1U_0402_25V6 for improve load response	2012/4/5	EVT
7		Modify CPU/GFX_CORE power circuit	0.1	41	Add PC45 330P_0402_50V7K, PC21 470P_0402_50V7K for EMI solution Add PC169 0.047I_0402_25V7K, change PR187 from 523 to 348_0402_1% change PR135 from 412 to 430_0402_1%	2012/4/5	EVT
8		Modify CPU/GFX_CORE power circuit	0.1	41	change PL14 from 0.22U_PCBM104T-R22MS_35A_20% to 0.22UH_MMD-10RCZ-R22M-28A (from H=3 to H=4) change PR201, PR152 from 27.4K to 61.9K_0402_1%, change PH4,PH5 470K_0402_5%(from Thinking to Panasonic) thermal issue	2012/4/5	EVT
9		Modify PROCESSOR DECOUPLING power circuit	0.1	42	Add PC74 330P_0402_50V7K, PC108 470P_0402_50V7K for EMI solution	2012/4/5	EVT
10		Modify DCIN/Pre-change power circuit	0.1	34	Sawp PC10 and PC301; Sawp PC14 and PC302	2012/4/5	EVT
11		Modify Battery CONN/OTP power circuit	0.1	35	Add PR105 0ohm to GND for BOM control (9012 H_PROCHOT#_EC) change PR61 from 21K to 21.5K and PR66 from 9.53K to 9.76K for 92 throttling and 56C recovery	2012/4/18	EVT
12		Modify Battery CONN/OTP power circuit	0.1	35	Delete PR78 and add PR61, PR63 for EC932, change PR66 from 9.53kohm to 9.76k ohm, OTP setting 92C thermal protection, 56C recovery	2012/4/26	EVT
13		Modify 3VALWP/5VALWP power circuit	0.1	37	Change PR56 from 402K to 100K for 3V/5V enable setting, Add PR53 for 3V/5V enable setting.	2012/4/26	EVT
14		Modify CPU/GFX_CORE power circuit	0.1	41	change PR187 from 348 to 324 for OCP 40A fine tune, change PC169 from 0.047U to 0.068U (RC match)	2012/4/26	EVT
15		Modify CHARGER	0.1	36	change PC22 from 0.1U_0402_25V6 to 330P_0402_50V7K	2012/5/2	EVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Modify Prochot# setting from KB9012 to G718(EVT MEMO introction)	0.2	35	change PR63 from 2.26K to 590 ohm, PR68 from 9.1 to 1.91K From 46.2W~38W to 42.8W~33.2W	2012/5/7	EVT
2		Modify Battery CONN/OTP power circuit Modify 3VALWP/5VALWP power circuit	0.2	35 37	Sawp PR81 and PR82 location leverage Mimic winsows	2012/5/17	DVT
3		Modify Battery CONN/OTP power circuit	0.2	35	Add PR111 between 3VLP and battery connect TH for EC932	2012/5/23	DVT
4		Remove PQ16 PC302 PR10 PR11	0.2	34	Remove 510N# RC, BATT+ to VS switch	2012/5/23	
5		MAINPWON double pull high.	0.2	35	Remove PR64	2012/5/23	
6		Modify 3v5v EN pin voltage (from 4.9V to 4.524V) for EN pin rating.	0.2	35	Change PR108 from 316K to 412K.	2012/5/23	
7		Modify 3v5v EN pin voltage for EN pin rating.	0.3	35	Change PR82 from 1000K to 887K.	2012/7/9	PVT
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